IKON MODEL 10085 REV. B

MULTIBUS*/HARDCOPY INTERFACE

February 1987

*MULTIBUS is a registered trademark of Intel Corporation

ikon corporation

2617 WESTERN AVENUE ● SEATTLE, WASHINGTON 98121 ● (206) 728-6465

IKON MODEL 10085 HARDCOPY INTERFACE

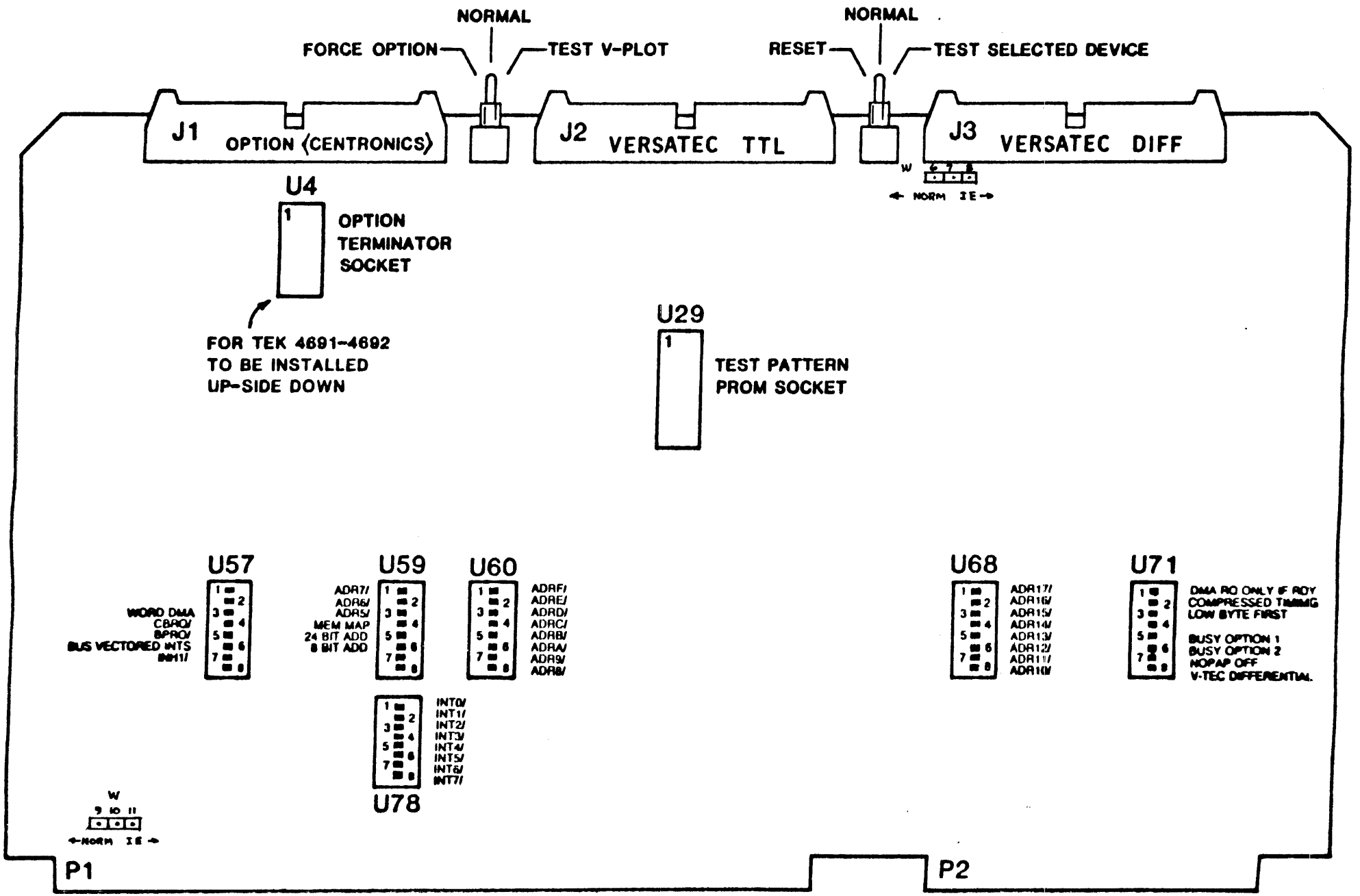


Table of Contents

Appendices

MODEL 10085 MULTIBUS/HARDCOPY INTERFACE

IKON CORPORATION

INCLUDES REVISION B

1. Introduction

The IKON Model 10085 Hardcopy interface is a high-performance DMA interface for hardcopy output devices including:

Versatec Electrostatic Plotters

Tektronix Color Copiers

Imagen Laser Printers

Other Centronics-compatible Devices

The 10085 is a fully hardware and software compatible emulation of IKON's popular 10071-5 Versatec interface, with the addition of an enhanced Centronics-type port (the option port) and several new operating modes. Software drivers written for the 10071-5 and Versatec combination will run without modification on the 10085.

The 10085 replaces the relatively slow MOS-LSI DMA controller IC used in the 10071-5 (and commonly found in other manufacturer's device interfaces) with an all-bipolar, delay-line-driven DMA mechanism. This bipolar, asynchronous DMA logic produces increased transfer rates and an improvement in bus efficiency (bus bandwidth used during DMA transfers) of two-to-one or greater when compared with the older design.

In addition to the 10071-5's word-only and byte-only DMA modes, the 10085 adds an optimizing addressing mode that can accept odd buffer addresses and odd byte range counts. DMA accesses are done in word mode for maximum bus efficiency

with the DMA logic discarding unwanted leading and/or trailing bytes.

The software selectable option port is a Centronics-type port with enhancements that take full advantage of the features of Tektronix color copiers. High current output drivers can drive any TTL-type load and termination including the Tektronix-preferred 95 ohm-to-ground coaxial-type termination. On-board receivers are all true Schmitt-triggers with socket-selectable terminations, and integrating R/C networks for maximum noise rejection.

Other option port enhancements include switch-selectable compressed timing and software-selectable "data streaming", both conforming to the Tektronix specification.

An enhancement of particular importance to field installation personnel is the ability of the 10085 to exercise the attached device and cable without cpu intervention. Operating a pair of board-edge mounted toggle switches can cause a test pattern (determined by an on-board PROM) to be sent to either the Versatec or option ports. The Versatec port may also be exercised in plot mode.

Revision A boards include a jumper option that allows masking off interrupts at power-up time.

2. General Specifications

Conforms to Multibus (IEEE-796) Specifications

Slave Mode Access

Switch selectable 8, 16, 20/24 bit address decode.

I/O or memory mapped.

Occupies 32 consecutive byte locations.

INH1/ drive capability.

Interrupts

All Multibus interrupt modes supported including bus-vectored interrupts.

DMA

All bipolar asynchronous DMA logic.

Drives all devices at full rated speed (burst rate approximately 1M-byte/second.

Bus cycles as short as 400ns/word.

8 or 16 bit data.

24 bit linear address generation.

Up to 128K byte blocks anywhere in address space.

Can handle odd buffer addresses and byte counts while doing 16 bit DMA transfers.

"Data streaming" capability for Tektronix color copiers.

Switch selectable byte ordering.

Device Interface

Diagnostic capability allows testing/exercising of device(s) and cable without cpu intervention.

Device test pattern determined by on-board PROM which may be custom tailored to device and user requirements.

CPU accessible diagnostic "hooks" allow exercising board and verifying driver software without device attached.

Directly supports all Versatec "Green Sheet" compatible products in both TTL and long-line (differential) modes. Long-line capability to 300 meters.

Supports any Centronics-compatible device.

High-current output drivers can dirve any TTL-type termination. Can source 30ma and sink 48ma.

Socketed input terminators allow matching device manufacturers preferred terminations.

All inputs received by Schmitt-triggers with R/C integration networks for maximum noise rejection.

Power and Environmental

Power consumption - 3A at 5VDC.

Commercial temperature range and humidity to 90% non-condensing.

3. On-Board Registers

The Model 10085 registers occupy a 32-byte block of addresses in the Multibus i/o or memory map (see Hardware Options for address and map selection). The low order five bits of the Multibus address bus are used to determine which on-board register is being accessed. The remaining address bits are examined to determine when the board is being addressed.

All registers except the p-i/o output register are 8 bits wide, aligned on word boundaries. Registers may be read and written in word or byte mode. During word writes the upper byte is ignored except when writing the p-i/o output register. During word reads the upper byte is not controlled.

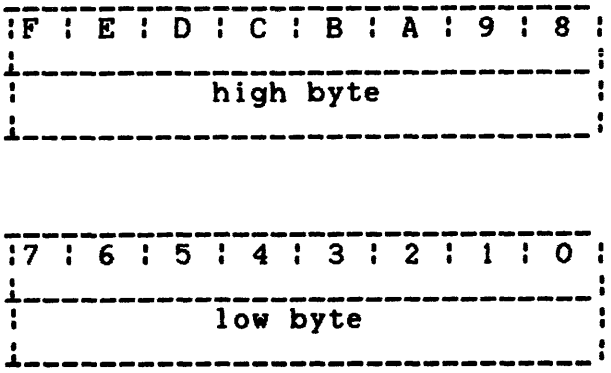
3.1. ON-Board Register Addressing

xxxx + 4 bits switch selectable -- all values in hex

Address	Write	Read
xxxx00	Mode	Status
xxxx02	Command	Diagnostic Command
xxxx04	P I-O Output	Diagnostic Data
xxxx06	DMA High Address	
xxxx08	8259A address 0	
xxxx0A	8259A address 1	
xxxx0C	DMA Mid and Low Address	
xxxx0E	DMA Range Count	
xxxx10		
xxxx12		
xxxx14	Start DMA	
xxxx16		
xxxx18	Clear First-Last F-F	
xxxx1A	Clear First-Last F-F	
xxxx1C	Start DMA	
xxxx1E	Start DMA	

3.2. Register Formats

Bit-numbering for all registers described in this manual is shown below. With one exception (the p-i/o output register) only the low order byte is used when accessing 10085 registers.



The term "option port" refers to the enhanced Centronics-type port available on the 10085.

Mode

An "O" in the Port column below indicates that the function of that particular command bit applies to the option port. A "V" indicates that the bit affects the operation of the Versatec port(s).

Bit	Name	Port	Function
7	TO	V	test ONLIN input
6	TN/IE	V/both	test NOPAP/enable interrupts
5	OP	both	select option port
4	DS	O	data streaming mode
3	OR	O	latched reset
2	OA	both	optimizing addressing mode
1	PL	V	plot mode
0	SP	V	simultaneous print-plot mode

All mode register bits are cleared to 0 by a bus initialize, MR in the command register, or the reset toggle switch.

TO Diagnostic. Forces the -ONLIN input low (true) when set to one. May be used to test this input and its associated interrupt. To be used only in TTL mode with plotter disconnected.

TN/IE Jumpers determine whether this bit tests the NOPAP input, or is a master enable bit for the on-board interrupt logic. See below and the interrupt and hardware options sections of this manual for details. 10085 boards prior to revision A provide the TN function only.

TN Diagnostic. Forces the NOPAP input low (false) when set to one. May be used to test this input and its associated interrupt. To be used only in TTL mode with plotter disconnected.

IE Configured by jumpers to be master interrupt enable bit. When set to 1 it allows the board to drive the selected Multibus interrupt line. Cleared to 0 by MR in the command register or by INIT/ on the Multibus.

OP Port select bit. 0 selects the Versatec port(s). 1 selects the option port. The port select toggle switch may also be used to force the selection of the option port by placing it in the "force option" position.

DS A 1 selects Tektronix-compatible data streaming mode for use with that manufacturer's color copiers. Allows an increase in throughput by eliminating normal handshaking within a data block. When data streaming mode is selected, any data byte sent to the device which has its MSB set to 1 leaves the interface ready to transmit the next byte without waiting for an ACK pulse from the device. Data bytes with their MSB set to 0 will cause the interface to wait for the ACK pulse. This feature will only function correctly when the connected device has been commanded to use data streaming.

Do not set this bit when the Versatec port is selected.

OR Latched reset bit. When set to one this bit causes the -INPUT PRIME signal to the option port to be asserted. It remains asserted until the OR bit is reset. This is useful when the option port device requires a reset signal longer than the 10085's normal 500ns pulse. This bit affects only the option port.

OA A 1 selects optimizing addressing mode for DMA transfers. It allows the interface to accept odd buffer starting addresses and byte counts while still doing DMA in word mode for maximum efficiency. (see DMA control).

PL 0 selects Versatec print mode. 1 selects plot mode.

SP 0 selects Versatec normal print-plot mode. 1 selects simultaneous print-plot mode.

Status

Bit	Name	Function
7	-OP	-option port selected
6	DR	device ready
5	IR	device and interface ready
4	DP	DMA not on and output buffer empty
3	PL/BY	print mode/busy
2	SP/FL	normal print-plot/fault
1	OL/SL	online/selected
0	NP/PE	no paper/paper empty

-OP 1 when the versatec port is selected. 0 when the option port is selected. Port selection (and this status bit) is controlled by the OP bit in the mode register and by the "force option" position of the port select toggle switch. The 10071-5 used this bit as a DMA IC type flag. Software written for early 10071-5 interfaces may have to be modified to ignore this bit--or use it a a port selection flag.

DR Indicates that the device is ready for data. Not interlocked with interface internal ready condition. To be used for diagnostic purposes only.

Versatec: 1 = -READY asserted.
Option: 1 = BUSY false and ACK received.

IR This is the master ready indication for all device and interface functions. When this bit is a one the interface and selected device are ready for the next device command, DMA block, or p-i/o output. Port switching should only be done when this bit is true, to avoid losing device ready synchronization when switching between two devices. Interface functions which do not result in data or commands being sent to the device (such as writing the DMA range count register) are always ready and do not require examining this bit.

Versatec: 1 = -READY input true, DMA not on, and data output buffer empty.
Option: 1 = BUSY false, ACK received, DMA not on, and data output buffer empty.

DP — A one indicates that a DMA block transfer is not in progress and that the output buffer (used by p-i/o and DMA) is empty. It is possible to start a new DMA block transfer or p-i/o output based on this bit alone--allowing an increased throughput since the new DMA transfer can be set up and enabled while the device is still processing previous data. This should only be attempted in very special situations since this bit is not interlocked with device ready--IR should be used in most cases since it also indicates that the Versatec (if selected) is ready for pulsed commands as well as data transfer. Most hardcopy raster-type applications are somewhat compute bound and using this bit as a transfer ready indication to attempt to improve performance will result in no actual increase in printing speed.

PL/BY
Versatec: 1 = print mode.
0 = plot mode.
Option: 1 = BUSY asserted.

SP/FL
Versatec: 1 = normal print-plot mode.
0 = simultaneous print-plot mode.
Option: 1 = -FAULT asserted.

OL/SL
Versatec: 1 = -ONLIN asserted.
Option: 1 = SLTC (selected) asserted.

NP/PE
Versatec: 1 = NOPAP (no paper) asserted.
Option: 1 = PE (paper empty) asserted.

Note: PL/BY and SP/FL switch only with the OP bit in the mode register. All other status bits switch ports with the OP bit or with the port select toggle switch. This allows using Versatec driver software written for IKON's 10071-5 Versatec interface to drive a device attached to the option port. When the "force option" position of the port select toggle switch is used, only those device signals which are equivalent for both ports are allowed to switch. The others, BUSY and -FAULT, are not available in the status register in this mode of operation, although the BUSY signal is used by the handshake logic when the option port is selected by either means.

Command

An "O" in the Port column below indicates that the function of that particular command bit applies to the option port. A "V" indicates that the bit affects the operation of the Versatec port(s).

Bit	Name	Port	Function
7	SA	both	software ACK
6			
5			
4	MR	both	master reset
3	VC	V	Versatec clear
2	VF	V	Versatec form feed
1	VT	V	Versatec remote EOT
0	VL	V	Versatec remote line terminate

All commands produce a pulse of approximately 500ns duration.

SA This command forces the internal device ready synch flip-flop to the ready state. Useful following possible error condition or after switching ports to make sure that the device and the internal ready flip-flop are synchronized. Also may be used to simulate an ACK pulse from the option device when that port is selected. Can be used to exercise the option port handshake logic.

MR Resets all interface logic. Sets all mode bits to 0. Selects the Versatec port, sets the ready synch flip-flop to the ready state, sends a -RESET pulse to the Versatec port and sends an -INPUT PRIME pulse to the option port.

VC Sends a -CLEAR pulse to the Versatec port.

VF Sends a -RFFED pulse to the Versatec port.

VT Sends a -REOTR pulse to the Versatec port.

VL Sends a -RLTER pulse to the Versatec port.

VF, VT, VL commands should not be issued unless IR in the status register is true.

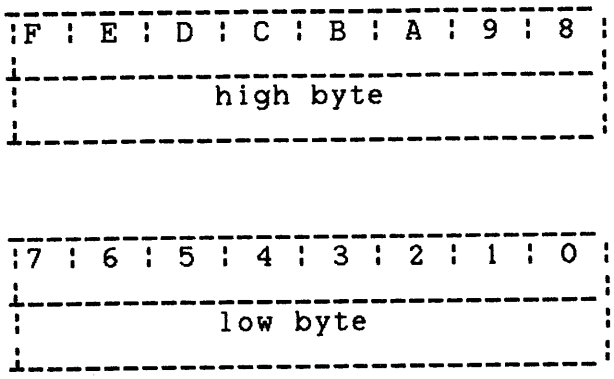
Diagnostic Command

Bit	Name	Function
7	0	
6	0	
5	0	
4	-VR	Versatec reset
3	-VC	Versatec clear
2	-VF	Versatec form feed
1	-VT	Versatec remote EOT
0	-VL	Versatec remote line terminate

This register contains the complement of the command(s) most recently sent to the Versatec port. Not cleared by bus INIT or MR in the command register.

The diagnostic command register is included for compatibility with IKON's 10071-5 Versatec interface. Its inputs are tied directly to the Versatec port's command drivers. It may be used to diagnose interface problems or to develop software drivers prior to attaching a plotter (and wasting a lot of paper).

P-I/O Output

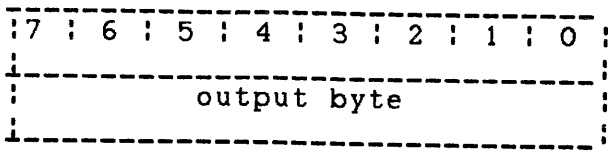


This is the only interface register directly accessible as a 16-bit word.

A write to this register will transmit one or two bytes to the selected port using the same handshake mechanism as DMA transfers.

If the interface is operating in normal word mode (10071-5 emulation), a write to this register will transmit both bytes to the Versatec port (or option port if forced by the port select toggle switch) in the order set by the byte order DIP switch. Please see "Switch Options" for location of this switch. If the interface is in any other operating mode--forced byte mode (DIP switch option), optimizing addressing mode, or the option port has been selected by the software, only the low order byte will be transmitted to the selected port.

Diagnostic Output



This register contains a copy of the most recent data byte sent to the Versatec port. Its inputs are physically connected to the Versatec TTL drivers. It may be used to verify their operation as well as test the DMA and p-i/o output mechanism, and interrupts.

When the Versatec TTL port is selected, reading this register also forces the incoming -READY line true. It remains true until reset by an outgoing data strobe to the Versatec port, or by a master reset. If DMA transfers have been enabled, repeatedly reading this port will allow examining the data as it would be sent to a plotter.

This should only be done in TTL mode with the plotter disconnected.

DMA High Address

The operation of this register is described in the DMA Control section of this manual.

8259A Address 0 & 1

The operation of these registers is described in the Interrupt Control section of this manual.

DMA Mid and Low Address, DMA Start and First/Last Control

The operation of these registers is described in the DMA Control section of this manual.

4. Interrupt Control

This interface supprorts all Multibus interrupt modes. It uses an on-board 8259A interrupt control IC which must be programmed for edge-sensitive operation. When bus-vectored interrupts are used, the on-board 8259A must be programmed to be a slave, and buffered mode must be selected. If non-bus-vectored interrupts are used, 8259A "single" mode should be selected, and the "POLL' command should be used to service interrupts.

Please see Appendix B for details of the 8259A interrupt controller IC.

The correspondence between the board's internal register address map and the 8259A's internal registers is shown below:

Address xxxx08 corresponds to 8259A A0 input = 0
Address xxxx0A corresponds to 8259A A0 input = 1

The proper sequence of commands to condition the on-board 8259A for non-bus-vectored operation (the interrupt scheme typically used by Multibus systems) is:

All values are in hex.

1) Write 12 to xxxx08
(ICW1, edge triggered, single, no ICW4)

2) Write a dummy value to xxxx0A
(dummy ICW2)

3) Write desired mask to xxxx0A
(note that a mask bit = 1 disables that interrupt level)

4)** For REV A boards that have the IE jumper option selected -- set the IE bit in the Mode register to 1 to allow the board to drive the selected Multibus interrupt line.

Upon receipt of an interrupt, the source is determined, and the interrupt reset by:

1) Write 0C to xxxx08
(condition 8259A for poll)

2) Read from xxxx08
(POLL)

The byte read will indicate the interrupting level in bits 2 - 0, and bit 7 will be a 1 if there is an actual interrupt pending.

After interrupt service is complete (or immediately following the POLL if interrupt nesting is allowed) the 8259A is released to process the next interrupt by:

Write 20 to xxxx08
(EOI command)

NOTE: Several of the possible interrupt conditions are controlled directly by the external device. It is possible that in extreme circumstances the condition causing an interrupt may have been removed before the software could service it. In this case, the byte read in the POLL operation will indicate a level 7 interrupt (spurious interrupt trap) and bit 7 will not be set. The controlling software should protect itself against this remote but possibly fatal possibility by always examining bit 7 after a POLL and ignoring interrupts that do not set this bit.

The interrupt conditions serviced by the on-board 8259A interrupt controller are:

8259A input	Versatec Port	Option Port
IR0	device and interface ready	
IR1	DMA off and p-i/o buffer empty	
IR2	device ready	
IR3	NOPAP asserted	PE asserted
IR4	-ONLIN de-asserted	SLCT de-asserted
IR5		-FAULT asserted
IR6		BUSY asserted
IR7	spurious interrupt trap	

IR0, 1, 2, 3, 4 switch with the OP bit in the mode register, or with the port select toggle switch.

IR5 and 6 switch only with the OP bit in the mode register.

The IR0 interrupt input is the most suitable for a DMA and interrupt or interrupt only mix of data and commands since

it is interlocked with all device and interface functions. An IR0 interrupt indicates that the interface and device are ready for both commands and data transfers.

The IR1 interrupt may be useful in some applications involving multiple DMA block transfers. A new DMA transfer may be started at any time after an IR1 interrupt, allowing maximum overlap of disk and hardcopy device DMA transfers. (actual transfers will begin when the device becomes ready). This interrupt is <u>not</u> interlocked with pulse commands to the Versatec port.

IR2 is included for diagnostic purposes and should not be used during normal operation.

NOTE: It is possible for the on-board 8259A to power up with its interrupt request line <u>ON</u>. Since the 8259A has no hardware reset input, it is important that the system software initialize the 8259A before enabling the Multibus interrupt line used by this interface.

If this is not done, unexpected interrupts may result.

Some computer systems have no provision for disabling Multibus interrupt lines during power-up and system boot. Revision A 10085 boards provide for this possibility by allowing the TN bit in the Mode register to be converted to a master interrupt enable bit (IE). This bit prevents the interrupt line from being driven until it is set to 1 by the driver software. The TN bit is converted to the IE by two sets of jumpers. See the Hardware Options section of this manual for details.

5. DMA Control

The somewhat unusual set of DMA control registers used by the 10085 emulates the operation of the 8237A-5 MOS LSI DMA control IC used by IKON's 10071-5 Versatec interface and is fully software compatible with drivers written for the 10071-5.

Three addressing modes are supported by the 10085: normal word mode, forced byte mode, and optimizing addressing mode. Normal word mode and forced byte mode are compatible with the 10071-5. Optimizing addressing mode provides greater programming and addressing flexibility and is recommended for new applications which do not require compatibility with the older interface.

All three modes use 8237-type access to the address and range counters. The range starting value and the lower 16 bits of the address starting value are broken into two bytes and passed in two transfers each through the byte wide data path to the DMA registers. The destination of data written to the DMA registers (and source of data read) is controlled by the first/last flip-flop which toggles after each access to xxxx0C or xxxx0E. The first/last flip-flop is initialized to point to the low-order byte of the address and range counters by bus INIT, MR in the command register, or a write of any value to xxxx18 or xxxx1A.

The buffer address referred to below is a 24-bit value which resolves addresses to the byte level: the lsb selects either of two bytes in a word.
The range count referred to below is a 16-bit count of the number of bytes to be transferred.

The procedure for starting DMA transfers in normal word mode is:

1) Write the high-order 8 bits of the buffer address to xxxx06.

2) Write a dummy value to xxxx1A to initialize the first/last flip flop.

3) Right-shift the low order 16 bits of the buffer address one bit position (normal word mode accepts only word addresses).

4) Write the low order byte of the resulting value to xxxx0C.

5) Write the high order byte of the value from step 3 to xxxx0C (shift right another 8 bit positions and write the low byte).

6) Write a dummy value to xxxx1A.

7) Right-shift the 16 bit range count one bit position (normal word mode accepts only word counts).

8) Subtract one from the resulting value.

9) Write the low order byte of the resulting value to xxxx0E.

10) Write the high order byte of the value from step 8 to xxxx0E (shift right another 8 places and write the low-order byte).

11) Write a dummy value to xxxx1C to start DMA.

DMA completion will be indicated in the status register and with an interrupt, if enabled.

Byte mode and optimizing addressing mode directly accept byte-oriented buffer addresses and range counts. Byte mode is intended for 8-bit systems that can't support word memory accesses. Optimizing addressing mode appears to the software as if it were operating in byte mode, but actually does memory accesses in word mode for maximum efficiency.

The procedure for starting DMA in byte or optimizing addressing mode is:

1) Write the high order byte of the buffer address to xxxx06.

2) Write a dummy value to xxxx1A to initialize the first/last flip-flop.

3) Write the low byte of the buffer address to xxxx0C.

4) Write the middle byte of the buffer address to xxxx0C.

5) Write a dummy value to xxxx1A to initialize the first/last flip-flop.

6) Subtract 1 from the range (byte) count.

7) Write the low byte of the resulting value to xxxx0E.

8) Write the high byte of that value to xxxx0E.

9) Write a dummy value to xxxx1C to start DMA.

DMA completion will be indicated in the status register and with an interrupt, if enabled.

DMA Address Register to Multibus Address Bit Mapping

Normal Word Mode (10071-5 emulation mode)

ADR0/ is forced to 0

xxxx06							
7	6	5	4	3	2	1	0
17/	16/	15/	14/	13/	12/	11/	10/

xxxx0C high							
7	6	5	4	3	2	1	0
	F/	E/	D/	C/	B/	A/	9/

xxxx0C low							
7	6	5	4	3	2	1	0
8/	7/	6/	5/	4/	3/	2/	1/

Bit numbers followed by a "/" represent Multibus address bits.

Forced byte and optimizing addressing mode

xxxx06							
7	6	5	4	3	2	1	0
17/	16/	15/	14/	13/	12/	11/	10/

xxxx0C high							
7	6	5	4	3	2	1	0
F/	E/	D/	C/	B/	A/	9/	8/

xxxx0C low							
7	6	5	4	3	2	1	0
7/	6/	5/	4/	3/	2/	1/	0/

Bit numbers followed by a "/" represent Multibus address bits.

6. Hardware Options

6.1. Switch Options

User selectable hardware options are controlled by DIP switches. The switch locations and layouts are shown below.

U57

1	
2	
3	off=byte on=word DMA
4	on=drive CBRQ/
5	on=serial bus pri.
6	on=bus vectored ints
7	on=drive INH1/
8	

U59

1	ADR7/
2	ADR6/
3	ADR5/
4	off=i/o on=mem map
5	off=16 on=24 bit map
6	off=16 on=8 bit map
7	
8	

U60

1	ADRF/
2	ADRE/
3	ADRD/
4	ADRC/
5	ADRB/
6	ADRA/
7	ADR9/
8	ADR8/

U68

1	ADR17/
2	ADR16/
3	ADR15/
4	ADR14/
5	ADR13/
6	ADR12/
7	ADR11/
8	ADR10/

U71

1	on=long data hold
2	on=fast option timing
3	off=high on=low byte first
4	
5	busy option 1
6	busy option 2
7	on=force NOPAP off
8	off=TTL on=diff Versatec

U78

1	INT0/
2	INT1/
3	INT2/
4	INT3/
5	INT4/
6	INT5/
7	INT6/
8	INT7/

6.2. Slave Addressing

The address of the board's register set is determined by switches at U59, U60, and U68.

The "ADRxx/" switches control the board's address within the i/o or memory map -- a switch set to **ON** will decode a **ONE** in that address bit position.

The width of the address bus decoded for slave access is controlled by switches U59-5 and -6.

width	U59-5	U59-6
8 bits	off	on
16 bits	off	off
24 bits	on	off

I/O or memory mappped slave access is controlled by switch U59-4.

off = i/o mapping
on = memory mapping

Most Multibus systems use a 16-bit i/o map and a 20- or 24-bit memory map. On-board pull-ups are provided which stabilize the upper four address bits at logic 0 for systems which only drive 20 address bits.

Note that all 24 address bits are driven when this board is bus master (DMA).

Multibus inhibit line INH1/ will be asserted whenever the board is addressed if switch U57-7 is **ON**. This is typically used when the board is to be in the memory map and will overlay a portion of RAM memory.

6.3. Interrupt Options

Interrupt Line Selection

Any of the eight Multibus interrupt lines may be selected by switches at U78. Only one switch at U78 should be on.

Vectored Interrupts

Switch U57-6 controls the connection of Multibus signal INTA/ to the on-board 8259A interrupt controller. This switch should be ON for bus-vectored operation and OFF for polled operation.

Polled interrupt mode is used in most Multibus systems.

Revision A -- Master Enable

On Revision A boards the TN bit in the Mode register may be converted to a master interrupt enable bit (IE) by changing two sets of jumpers. One set of jumpers is located at the pin 1 end of the P1 Multibus connector. The other is located adjacent to the reset/test toggle switch. Both jumper sets must have a jumper clip installed, and both clips must be installed in the same position.

If the clips are installed in the "NORM" postiion, the board will function identically to older boards (prior to REV A) and the TN bit will be available to test the NOPAP Versatec input. If the clips are installed in the "IE" position, the TN bit is converted to the IE (interrupt enable) bit, and the on-board 8259A interrupt control IC will be prevented from driving the selected Multibus interrupt line until this bit is set to 1 by the driver software. This feature can be used to prevent the board from issuing an unexpected interrupt during power-up or system boot.

NOTE The "IE" mode is not software compatible with older boards.

6.4. DMA Options

Word/Byte

Switch U57-3 enables the 10085 to do word mode DMA accesses. It should be ON for normal word mode (10071-5 emulation) and optimizing addressing mode, and OFF for forced byte mode operation. This switch also affects the number of bytes transmitted when using the p-i/o output register. If it is OFF only one byte will be transmitted in a p-i/o output operation. If it is ON the number of bytes transmitted depends on addressing mode and port selected. (see mode register description).

Byte Ordering

If switch U71-3 is OFF the high order byte of a DMA or p-i/o output word will be transmitted to the device first. If is is ON the low byte will be sent first.

Bus Request

Switch U57-4 set ON will cause the Multibus request line CBRQ/ to be driven during a DMA request. Most systems require that this line be driven.

Serial/Parallel Priority

Switch U57-5 set ON causes the Multibus priority line BPRO/ to be driven during a DMA request. This switch should be ON for serial bus arbitration, and OFF for parallel arbitration.

DMA Request on Ready or Buffer Empty

When switch U71-1 is ON the 10085 will request DMA accesses only when the selected device is ready. If this switch is OFF DMA accesses will be requested as soon as the data buffer is empty, allowing overlap of DMA requests with the device's processing of the previous byte.

NOTE: The Versatec "Green Sheet" specification requires that data from a previous transfer be held valid until the plotter becomes ready--requiring that this switch be ON. In fact, all existing Versatec products do not require that data be held beyond the trailing edge of the data strobe. In general, this switch may be OFF with the caution that future Versatec products may require it to be ON. The option port will meet the Centronics or Tektronix

specification with the switch in either position, but somewhat greater throughput will be achieved with the switch OFF when connected to a high-speed device.

6.5. Port Options

TTL/Differential Versatec Only

If switch U71-8 is OFF the Versatec TTL port is selected (and the plotter cable should be plugged into J2). If it is ON the Versatec differential port (J3) is selected. ON also prevents a read of the diagnostic data register from forcing the Versatec -READY line low, and disables the drivers for the TO and TN bits in the mode register.

Most V80 plotters use the TTL interface. Many wide-bed plotters are differential. Determine the interface scheme used by the plotter before connecting to the 10085.

NOPAP Disable Versatec Only

Setting switch U71-7 ON holds the Versatec NOPAP status input low (false). This switch should only be set ON when the Versatec differential port is enabled--it prevents a false NOPAP indication (NOPAP is not driven by the plotter in differential mode).

Busy Options 1 & 2 Option Port Only

Switches U71-5 and -6 determine how the option port status input BUSY is used in the device ready equation. If U71-5 is ON the device will be considered not ready by the handshake logic whenever BUSY is asserted. If U71-6 is ON the device will be busy from the leading edge of BUSY until the trailing edge of ACK (which requires that BUSY be removed before the trailing edge of ACK). If neither switch is ON BUSY is not used in the ready equation.

In any case, the device is also considered not ready from the leading edge of the data strobe until the training edge of ACK. Both switches should be OFF for devices which do not drive BUSY, and when exercising the option port with no device attached since a floating BUSY input will appear to be asserted.

***** Busy option 2 (U71-6) is provided only as a hedge against a really bizarre interpretation of the Centronics specification (there are many!) and should NOT be used under normal circumstances. IN 99.999% of 10085 installations, the correct switch setting will be U71-5 ON U71-6 OFF.

Compressed Timing Option Only

When switch U71-2 is OFF the data transfer timing of the option port conforms exactly to the Centronics specification--1us data set-up and hold, and 1us data strobe. When this switch is ON a Tektronix-type compressed timing is used--200ns data set-up and hold, and 800ns data strobe. Compressed timing is made available for the Tektronix 4691 and 4692 color copiers, which can take advantage of the somewhat higher throughput possible with this timing.

6.6. Option Port Terminations

The socket at U4 holds a resistor DIP that provides the termination for the option port input signals. The resistor network chosen depends on the requirements and capabilities of the device being driven.

Devices with low drive capabilities (true Centronics compatible devices) will require a 470ohm or 1kohm resistor DIP that has all internal resistors tied to pin 16 (vcc).

Whenever the device has sufficient drive (is able to sink 25ma) a 220/330ohm resistor DIP is preferred. This provides a much better match to most cables and will reduce ringing and cross-talk.

Most Tektronix color copiers--other that the 4695 which uses Centronics-type terminations--will work best with a 100ohm resistors to ground. This is accomplished by installing a DIP that has 100ohm resistors tied to pin 16 UPSIDE-DOWN in the terminator socket. Right-side-up resistor DIPs have pin 1 in the upper left hand corner (closest to the U4 label).

Tektronix color copiers have several driver/receiver and termination options. It is important that the customer verify that the 10085 and color copier set-up agree.

NOTE: The 10085 is normally shipped with a 220/330ohm terminator installed at U4. 100ohm and 470ohm terminator DIPs are available in the "spare terminator" sockets at UX1 and UX2.

6.7. Input Signal Filtering

All device input signals are provided with true Schmitt-trigger receivers and R/C integration networks for maximum noise rejection (particularly important when using light Centronics-type terminations with a high-speed device). The integration time (maximum noise pulse rejected) is given by the approximation:

$$T = R*C$$ where T is in nano-seconds, C is in pico-farads, R = 2.2

The 10085 is shipped with 220pf capacitors for all integrators. This is the maximum allowable value which can be used on the Versatec port -READY input--greater integration times may reject legitimate pulses. All other inputs on both

ports can tolerate much larger capacitance values (up to 2000pf or so).

While the factory-supplied capacitors will be adequate for almost all installations, it is possible that extreme conditions or special devices may require a different integration time. Contact IKON for assistance in locating and changing the appropriate on-board capacitors.

7. Device Exerciser

7.1. Exercise/Test Procedure

The IKON model 10085 provides a convenient means of exercising an attached device and verifying cable connections and device and interface set-ups. An on-board PROM contains two test patterns--one for the Option port, and one for the Versatec port(s)--which may be used to exercise the attached devices without CPU intervention.

When the "reset-test" toggle switch (located at the board edge between the Versatec TTL and differential connectors) is moved to the "test" position (toward the differential connector) a PROM-driven repeating test pattern is sent to the selected device. Testing is terminated by moving the "reset-test" switch to the "reset" position and back to the center-off position.

The Versatec port (TTL or differential as determined by switch U71-8) is selected by bus INIT or by resetting the board with the "reset-test" toggle switch. The option port may be manually selected for exercising by moving the "port select" toggle switch (located between the option and Versatec TTL connectors) to the "force option" position (toward the option connector). If the software is to determine port selection, or if the software expects the Versatec port to be the default port, this switch must be returned to its center-off position after the device exercise process has been completed.

7.2. Versatec Plot Mode Testing

If the "port select" toggle switch is moved to its extreme right position--"test plot"--prior to starting the device test, the Versatec port will be selected, the PRINT signal to the Versatec will be de-asserted (PLOT mode), and an all-ones pattern will be sent to the plotter causing an all-black plot to be produced. This is particularly useful for some wide-bed plotters that do not include character generators.

7.3. Test Pattern PROM

The test/exercise pattern sent to the device is determined by a PROM installed at U29 and the position of the "port select" toggle switch. When the Versatec port(s) are selected, the test pattern is taken from the high 256 bytes of the PROM. When the Option port is selected, the test pattern is taken from the low 256 bytes of the PROM. The test patterns in PROM are normally the same: a banner and an ASCII test pattern, allowing exercising of Versatec products in print mode and Centronics compatible products as if they were printers. For Centronics-type devices that do not have a line printer emulation mode, or when it is desirable to exercise some specific feature of the Option port device, a special test pattern PROM may be specified.

Special test patterns also be generated which include customer identification, such as city of manufacture, or product type. The exact test pattern will depend on device characteristics and customer requirements.

Please see Appendix H for a listing of available test PROMs and devices supported.

Contact IKON for additional information on available test pattern PROMs and custom pattern specification.

8. Option Port Signal Description

-STROBE output

-STROBE is a negative pulse of 1us (normal timing) or 800ns (compressed timing) that indicates to the external device that data is present on the data lines.

DATA1--DATA8 output

The data lines are positive true signals that carry the data to be transmitted to the external device. DATA8 is the most significant bit. The data lines are stable for 1us (normal timing) or 200ns (compressed timing) before and after -STROBE.

-ACKNLG (ACK) input

This is a response to the -STROBE signal. It is a negative pulse and may be of any duration greater than 200ns. The interface considers the device to be not ready from the leading edge of -STROBE until the trailing edge of -ACKNLG. Once this ACK pulse has been received the interface may transmit another byte of data unless BUSY is asserted.

BUSY input

BUSY is a positive-true indication from the device that it is not ready to accept data. -STROBE will not be issued when BUSY is true. A switch option causes the interface to ignore BUSY for special applications.

The assertion of BUSY may be enabled to cause an interrupt.

PE input

PE (paper empty) is a positive-true status input from the device. Its meaning is device dependent.

The assertion of PE may be enabled to cause an interrupt.

SLCT input

SLCT (selected) is a positive-true status input from the device. Its meaning is device dependent.

The de-assertion of SLCT may be enabled to cause an interrupt.

-FAULT input

-FAULT is a negative-true status input from the device. Its meaning is device dependent.

The assertion of -FAULT may be enabled to cause an interrupt.

-INPUT PRIME output

This negative-true output is used to reset the external device. It is generated by a Multibus INIT/ signal, by the MR bit in the command register, or by the OR bit in the mode register. When generated by the MR bit, -INPUT PRIME is a pulse approximately 500ns long. The latched OR mode bit may be used to extend this signal for any duration for devices that require a longer reset pulse.

TEKTRONIX, INC
Beaverton, Oregon

APPENDIX A

INSTALLATION GUIDE

IKON 10085 MULTIBUS/HARDCOPY INTERFACE
For
APOLLO DSP80/DN400 SERIES TERMINAL NODES
WITH TEKTRONIX 4690 SERIES COLOR COPIERS

APPENDIX A

INSTALLATION GUIDE

The following installation guide was written specifically for Tektronix color copiers when used with the 10085 Hardcopy interface installed in an Apollo computer. It should serve as an example when using the 10085 to interface other hardcopy devices to Apollo computer systems, or when installing the 10085 in other manufacturer's computers.

In particular, this installation guide may be followed exactly when the 10085 is used to interface Versatec products to Apollo nodes. The only additional consideration when attaching Versatec plotters to this interface is whether the plotter uses TTL or differential interfacing. (See the Port Options section of this manual). The U4 terminator DIP is not used by the Versatec portion of the 10085.

In addition to the normal ASCII test pattern available at the Versatec port(s), plot mode may also be exercised. (See the Device Exerciser section of this manual).

Consult Ikon for installation instrucions for other devices and computers.

CONTENTS

INTRODUCTION

INTERFACE DESCRIPTION

The high performance IKON 10085 Multibus*/Hardcopy Interface for hardcopy peripheral devices interfaces a TEKTRONIX 4690 Series Color Graphics Copier with an Apollo DSP80 or DN400 Series Terminal Node. The Interface includes an all-bipolar delay-line-driven DMA mechanism that supports raster-type hardcopy devices.

The software-selectable Option Port of the 10085 Interface provides high output drive capability and takes full advantage of the features of Tektronix color copiers. Option Port enhancements include switch-selectable compressed timing and software-selectable "data streaming," both of which conform to the Tektronix Parallel Interface Specification -- 469X Color Copiers and Color Graphic Terminals (GPP Specification No. 15-005).

COMPATIBILITY WITH TEKTRONIX COLOR COPIERS

The 10085 Interface is compatible with the 4691, 4692, and 4695 Color Graphics Copiers but requires certain variations in the Option Terminator and Test Pattern PROM installation for the 4695. The installation procedure in this appendix flags these differences and gives alternate instructions.

RELATED DOCUMENTATION

For further copier information, consult Table A-1 for the part numbers of related Tektronix documentation.

* Multibus is the registered trademark of Intel Corporation.

Table A-1

TEKTRONIX PART NUMBERS OF 4690 SERIES COPIER MANUALS

TYPE OF MANUAL	4691	4692	4695
Operators	070-4500-00	070-4816-00	070-4646-00
Service	070-4498-00	070-4815-00	070-4645-00
Device Driver Development Guide	070-4547-00	070-4818-00	070-4990-00

INSTALLATION

UNPACKING THE INTERFACE

Unpack the IKON 10085 device, and identify the following items:

- Multibus Interface circuit board
- 34 -conductor ribbon cable
- IKON Instruction manual
- Alternate Option Port Terminator (U4 socket)
- Alternate Test Pattern PROM (U29 socket)
- Checklist showing factory switch settings

PRELIMINARY STEPS

If the node is powered up, then:

1. Indicate by normal procedures to any other users locked onto the same node as you that you plan to shut down the node. This courtesy avoids inconveniencing others with an unannounced shutdown.
2. Press the CMD (command) button on the terminal keyboard's small keypad.
3. Type SHUT on the terminal keyboard in your system. This saves any pending files, and executes logoff with a graceful shutdown.
4. Shut down the node completely by doing the steps in Table A-2.

Table A-2

POWER-DOWN PROCEDURE

NODE SERIES	STEPS TO SHUT DOWN THE NODE
DN400	1. Press the red POWER ON rocker switch (front panel) to the off position, causing the green POWER DOWN indicator to come on. See Figure A-1. 2. Push the toggle-type main power switch (rear panel) down to the OFF position. See Figure A-2.
DSP80	Push the rocker-type main power switch (rear panel) to the OFF position. See Figure A-2. There is no separate power-on switch such as on the DN400 Series.

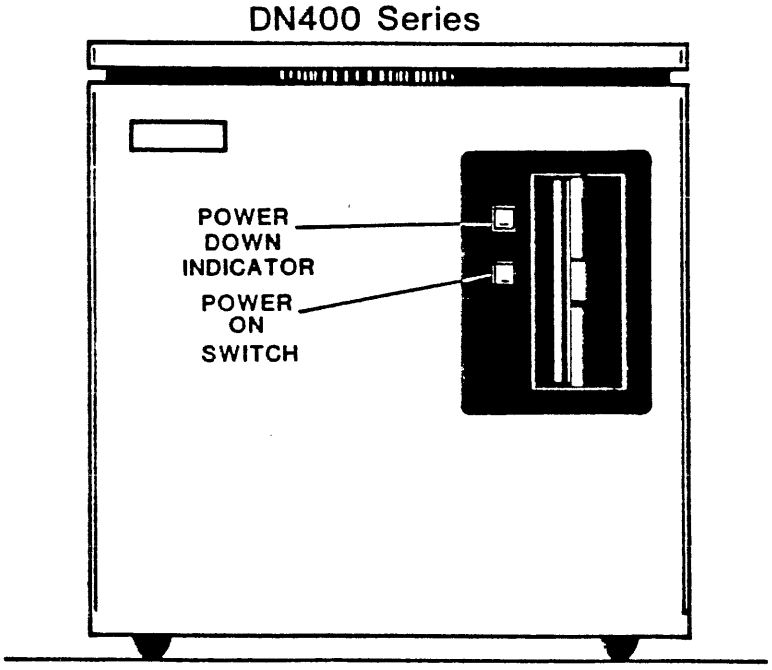


Figure A-1. Front Panel POWER ON Switch and POWER DOWN Indicator.

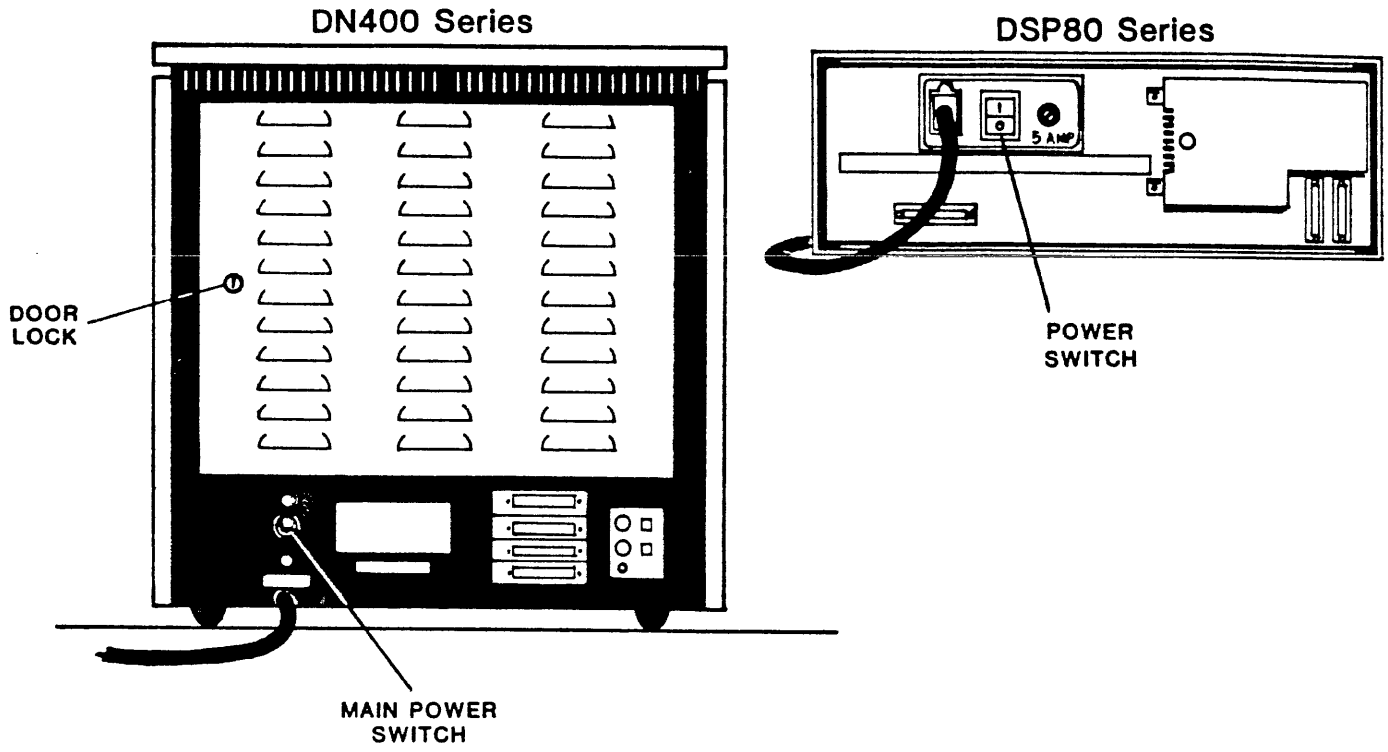


Figure A-2. Rear Panel Main Power Switch.

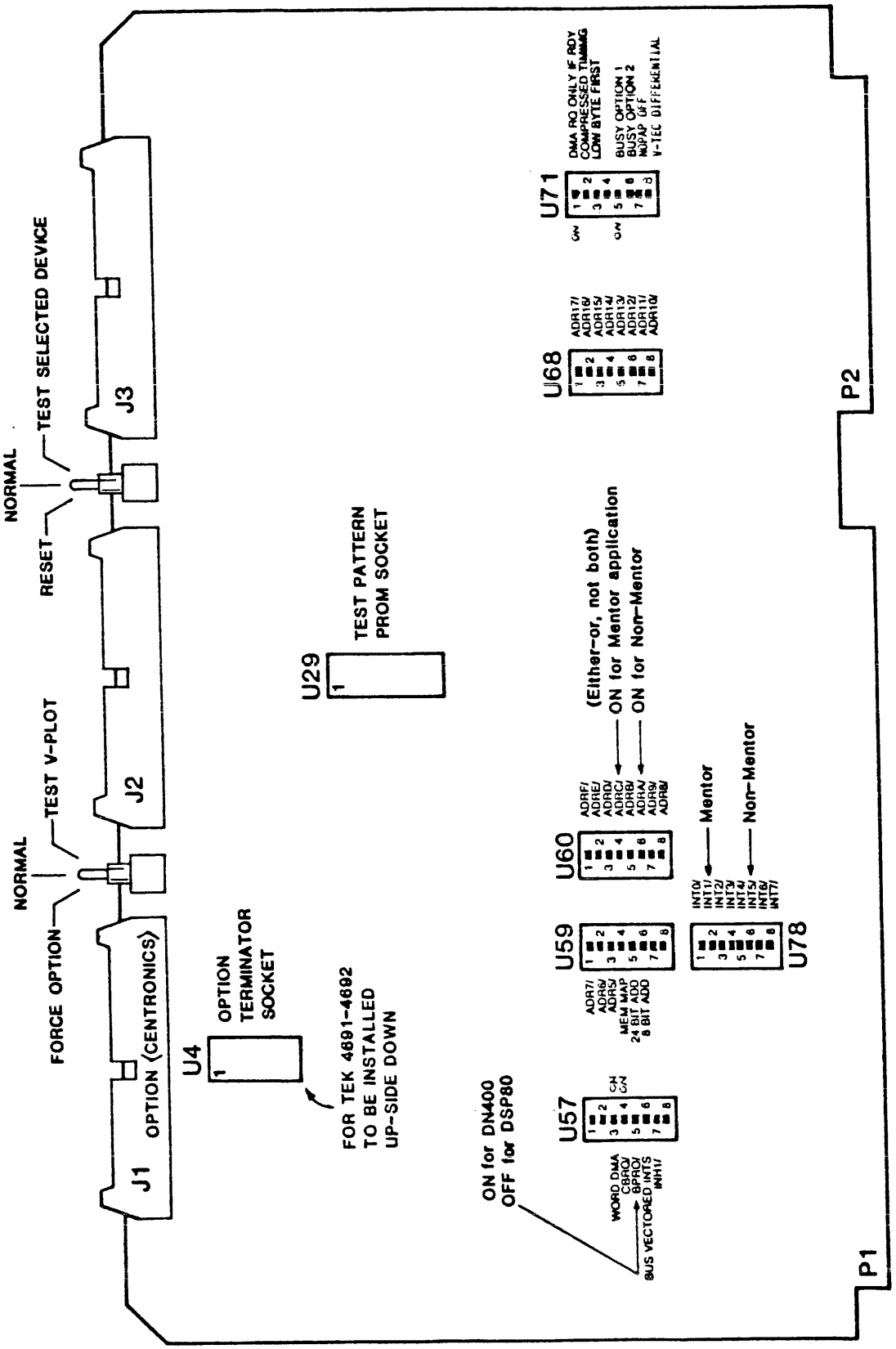


Figure A-3. Circuit Board Switches and Sockets.

SETTING BOARD SWITCHES AND CHECKING SOCKETS

On the Multibus Interface circuit board, set the 8-segment DIP switches and check the U4 and U29 sockets before you install the board in the card cage, as indicated in the following procedures (refer to Figure A-3).

NOTE

The factory setting of Interface board switches is based on a standard configuration with a 10-ft Centronics-style ribbon cable unless specified otherwise when ordered. In the case of using a cable longer than 10 feet for a 4691 or 4692 Copier, refer to the Operators Manual for the particular copier.

U71 DIP Switch

- Set Switch 1 (DMA RQ ONLY IF RDY) to the ON position.
- Set Switch 5 (BUSY OPTION 1) to the ON position.
- Setting Switch 2 (COMPRESSED TIMING) is optional for a 4691 or 4692 Color Copier (nominal 1200 nsec/byte timing). The benefit of compressed timing, with Switch 2 ON, is a somewhat increased throughput. Compressed timing is not needed for a 4695 Color Copier (nominal 3 usec/byte timing). The recommended normal setting is Switch 2 OFF.
- Leave the remaining switches (other than the above) in their factory-set position unless a conditional note in this manual or in related documentation indicates otherwise.

U57 DIP Switch

- Set Switch 3 (WORD DMA) to ON position.
- Set Switch 4 (CBRQ/) to ON position.
- Set Switch 5 (BPRO/) to OFF position for the Apollo DSP80 Series, but to ON position for the Apollo DN400 Series.

NOTE

For the DSP80 series, the CCLK strap (located in the DSP80 logic) must be ON.

- Leave the remaining switches (other than the above) in their factory-set position unless a conditional note in this manual or in related documentation indicates otherwise.

NOTE

The following switch settings for U60 and U78 apply only to current software. Future Mentor/Apollo software revisions might require different switch settings.

U60 DIP Switch

- Set Switch 4 (ADRC/) to the ON position for Mentor application or to the OFF position for non-Mentor application.
- Set Switch 6 (ADRA/) to the ON position for non-Mentor application or to the OFF position for Mentor application

NOTE

Switches 4 and 6 are mutually exclusive; that is, either Switch 4 or Switch 6 is ON but not both. For Mentor application, set 4 to ON and 6 to OFF; for non-Mentor, set 6 ON and 4 OFF.

- Leave the remaining switches (other than the above) in their factory-set position unless a conditional note in this manual or in related documentation indicates otherwise.

NOTE

Special conditions, such as the installation of multiple 10085 Interfaces in the same node, might require other switch settings.

U78 DIP Switch

- Set Switch 2 (INT1/) to the ON position for Mentor application or to OFF for non-Mentor application.
- Set Switch 6 (INT5/) to the ON position for non-Mentor application or to OFF for Mentor application.

NOTE

Switches 4 and 6 are mutually exclusive; that is, either Switch 2 or Switch 6 is ON but not both. For Mentor application, set 2 to ON and 6 to OFF; for non-Mentor, set 6 ON and 2 OFF.

- Leave the remaining switches (other than the above) in their factory-set position unless a conditional note in this manual or in related documentation indicates otherwise.

Summary of DIP Switches

Use Table A-3 as a checklist for double-checking all switch settings.

Table A-3

DIP SWITCH SETTINGS

SWITCH	SWITCH NAME	OFF	ON*
U57-1			
-2			
-3	WORD DMA		X*
-4	CBRQ/		X
-5	BPRO/	DSP*	DN*
-6	BUS VECTORED INTS	X	
-7	INH1/	X	
-8			
U59-1	ADR7/	X	
-2	ADR6/	X	
-3	ADR5/	X	
-4	MEM MAP	X	
-5	24 BIT ADD	X	
-6	8 BIT ADD	X	
-7			
-8			
U60-1	ADRF/	X	
-2	ADRE/	X	
-3	ADRD/	X	
-4	ADRC/	NON*	MEN*
-5	ADRB/	X	
-6	ARDA/	MEN	NON
-7	ADR9/	X	
-8	ADR8/	X	

* Legend:
X: indicates ON/OFF state, per column head.
DN: indicates ON/OFF state for DN400 Series, per column head.
DSP: indicates ON/OFF state for DSP80 Series, per column head.
MEN: indicates ON/OFF state for Mentor application, per head.
NON: indicates ON/OFF state for non-Mentor application.

Table A-3 (cont)

DIP SWITCH SETTINGS

Switch	Switch Name	OFF	ON*
U68-1	ADR7/	FS	
-2	ADR6/	FS	
-3	ADR5/	FS	
-4	ADR4/	FS	
-5	ADR3/	FS	
-6	ADR2/	FS	
-7	ADR1/	FS	
-8	ADR0/	FS	
U71-1	DMA RQ ONLY IF RDY		X
-2	COMPRESSED TIMING		OPT*
-3	LOW BYTE FIRST	X	
-4	TEST PATTERN SELCT	TBD*	
-5	BUSY OPTION 1		X
-6	BUSY OPTION 2	X	
-7	NOPAP OFF	VER*	
-8	V-TEC DIFFERENTIAL	VER	
U78-1	INT0/	X	
-2	INT1/	NON	MEN
-3	INT2/	X	
-4	INT3/	X	
-5	INT4/	X	
-6	INT5/	MEN	NON
-7	INT6/	X	
-8	INT7/	X	

*Legend:
X: indicates ON/OFF state, per column head.
FS: indicates "however set at factory" (see packing sheet).
OPT: indicates "optional" (see U71 paragraph above).
TBD: indicates "to be determined."
VER: applies to Versatec attachment only. Tek copiers don't care.
MEN: indicates ON/OFF state for Mentor application, per head.
NON: indicates ON/OFF state for non-Mentor application, per head.

Checking the Option Terminator (U4)

Refer to Figure A-3 to locate the U4 socket on the 10085 Interface board, and verify that the appropriate Option Terminator is installed, as follows:

- When interfacing with the 4695 copier, use the 470-Ohm Option Terminator (CTS #761-1-R470) in the U4 socket.

- When interfacing with the 4691 or 4692 copier, install the 100-Ohm Option Terminator (CTS #761-1-R100) upside-down in U4 to use the optional long cables. Use the 470-Ohm Option Terminator (CTS #761-1-R470) for a standard short-cable configuration.

CAUTION

The cable drive option must match the cable terminations in the 4691 or 4692. When using the 100-Ohm terminator, be sure to install it upside-down in U4.

If the proper terminator for your node-copier system was not factory installed, locate the alternate terminator supplied in the Interface package.

Checking the Test Pattern PROM (U29)

Refer to Figure A-3 to locate the U29 socket on the 10085 Interface board, and verify that the appropriate Test Pattern PROM is installed in the correct position, as follows:

- When connected with a 4695 copier, the Interface board requires the [to be determined] PROM in U29.

- When connected with a 4691 or 4692 copier, the Interface board requires the [to be determined] PROM in U29.

INSTALLING THE INTERFACE CIRCUIT BOARD

1. Access the card cage.

   DN400 Series: Access the vertical circuit-card cage on a DN400 Series node (see Figure A-4) by unlocking and opening the rear door about 90 <degrees>. (To remove the door, raise the opened door until it clears the hinge pin.)

   DSP80 Series: Access the horizontal card cage of a DSP80 Series node (see Figure A-4) by snapping off the front cover (no catches or screws).

2. Install the board.

   DN400 Series: Carefully insert the Interface board, with the J1 Option Port at the top and the board components on the left side, into the card cage's second slot from the right, next to the PNA board.

DSP80 Series: Carefully insert the Interface board into any open slot of the upper section of the card cage, with the J1 Option Port to the right (as viewed by technician when inserting board in slot) and with the component side of the board facing up.

3. With the board ejector tabs retracted to their non-extended installation position, push the Interface board all the way into the card cage until the board edge-connectors seat firmly into the backplane.

CONNECTING THE INTERFACE RIBBON CABLE

1. Take in hand the ribbon cable that interconnects the Interface board's Option Port to one of the copier ports. Notice that the 34-pin connector on the "node end" of the cable has plastic snap catches, and the 36-pin connector on the "copier end" has holding screws to secure it to a copier port connector. You can install the cable only one way.

2. Connect the cable's "snap-catch" connector to the Interface board's J1 connector, and the cable's "screw-grip" connector to one of the available ports on the copier rear panel, according to the orientation of Step 1. See Figure A-5.

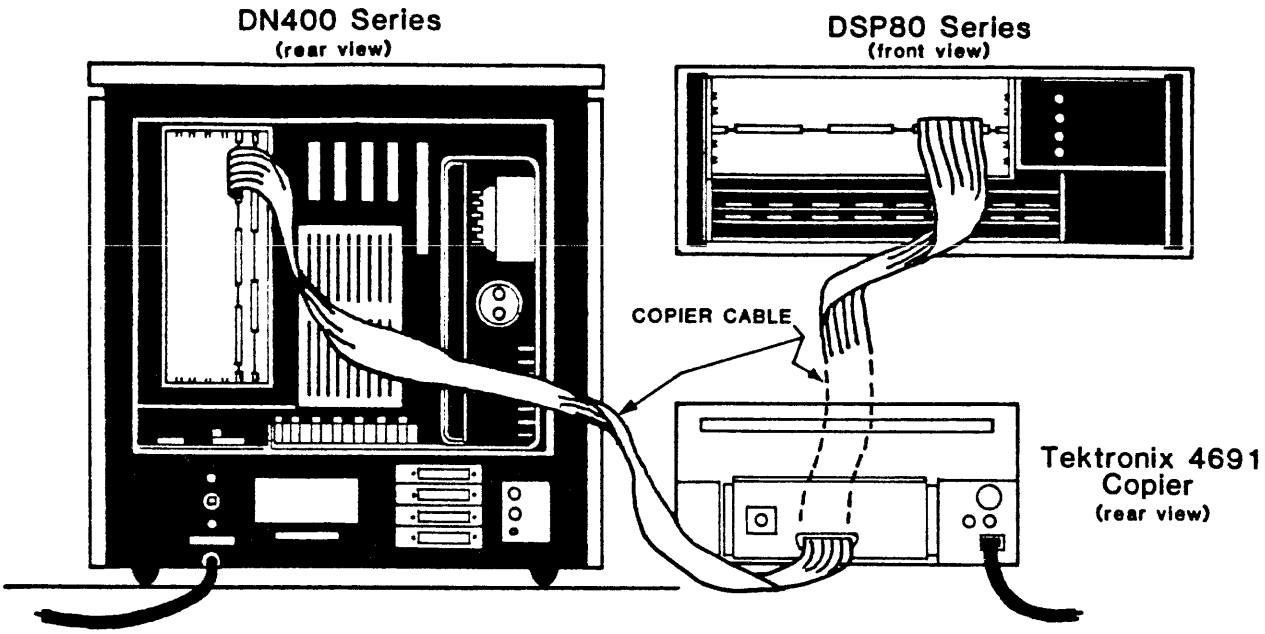


Figure A-5. Node-to-Copier Cabling.

TERMINATION STRAPS ON 4691 PARALLEL INTERFACE BOARD

The 4691 Parallel Interface board provides for termination selection. This is accomplished by moving three jumper straps and one resistor network package. Jumper positions labeled "LONG" implement **parallel** termination. The jumper positions labeled "SHORT" implement **series** termination. See Figure A-6.

CAUTION

It is important to keep host and copier termination selection the same, or else severe signal degradation may occur.

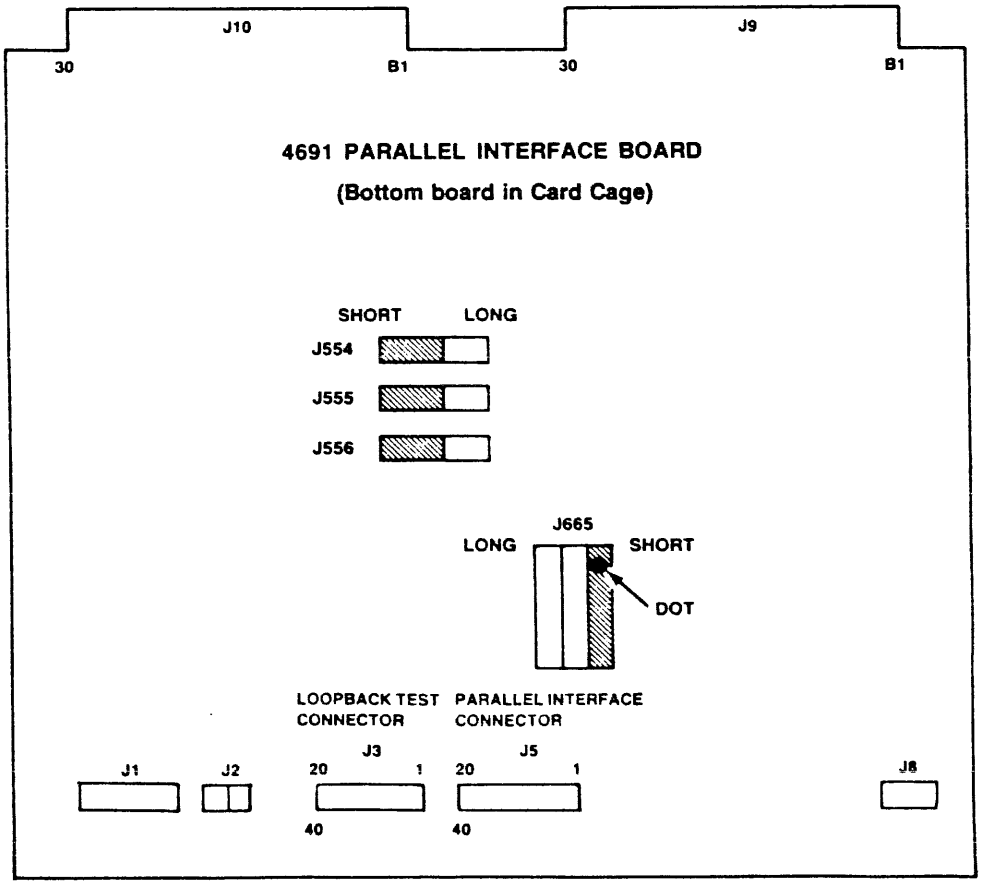


Figure A-6. 4691 Parallel Interface Connectors and Terminations.

TERMINATION STRAPS ON 4692 PARALLEL INTERFACE BOARD

The 4692 Parallel Interface board provides for termination selection. However, changing the termination is a somewhat complicated procedure. Call your local Tektronix service representative, or at least consult the 4692 Service Manual. (We recommend the former alternative.)

POWER UP AND TEST PATTERN

After prescribing a readiness check, this section describes the following procedures:

- Powering Up the Node and Copier
- Toggling the Option Port Switch
- Running a Test Pattern

READINESS CHECK

Before you power up the instruments and attempt a test pattern hardcopy, review this checklist to ensure that the Ikon 10085 Multibus/Hardcopy Interface is fully and properly installed, as previously detailed in this manual.

[ ] Proper setting of all DIP switches on Interface board
[ ] Insertion of proper Option Terminator in U4
[ ] Insertion of proper Test Pattern PROM in U29
[ ] Installation of Interface board in circuit card cage
[ ] Installation of Interface cable between node and copier

POWERING UP THE NODE AND COPIER

The following Power-Up procedures assume that the instruments' power cords are already plugged into an ac power source, per installation instructions.

Apollo DN400 Series Node Power-Up

1. Toggle the rear-panel main power switch to the ON position (see Figure A-2). This accesses the ac power source.
2. Press the front-panel POWER UP rocker switch to ON position (see Figure A-1). This activates the internal circuitry.

Apollo DSP80 Series Node Power-Up

Press the DSP80 Series rear-panel rocker switch to the ON position to power up the node.

Tektronix Color Copier Power-On

Activate the POWER ON condition for the particular copier model, per Table A-4, by pushing the ON switch.

Table A-4

COPIER POWER-ON SWITCHES

COLOR COPIER	SWITCH LOCATION	TYPE OF SWITCH
4691	Front panel	Push Button (latch type)
4692	Front panel	Push Button (non-latch)
4695	Left side	Rocker switch

SETTING THE OPTION PORT SWITCH

Move the edge-mounted toggle switch (between J1 and J2 on the Interface board, see Figure A-3) to the FORCE OPTION position. This activates the J1 Option Port to allow the processing of hardcopies.

> [EDITORIAL NOTE: The hardware switch overrides the current Mentor software. Future software probably will not use the FORCE OPTION switch. The FORCE OPTION switch allows you to drive the Tektronix copier with Versatec software. This will not be the preferred approach when full software support is available.]

RUNNING A TEST PATTERN

Move the RESET/TEST switch (between J2 and J3 on the Interface board, per Figure A-3) to the TEST SELECTED DEVICE position to activate a test pattern routine. When the node is connected to a 4695 copier, the copier repeatedly receives the 64-character ASCII character set (see Figure A-7 for a sample hardcopy). *

To exit the test mode, move the RESET/TEST switch to the RESET position (which resets the interface and the device. When you release this spring-loaded switch lever, it automatically returns to the NORMAL (center) position. This terminates the test pattern routine.

IF IT DOESN'T WORK, WHAT THEN?

If the node does not transmit a test pattern to the copier, or if the generated test pattern is unsatisfactory, contact your IKON representative for assistance.

* Other test pattern PROMs will be made available to exercise various Textronix color copiers. Contact IKON for PROM availability.

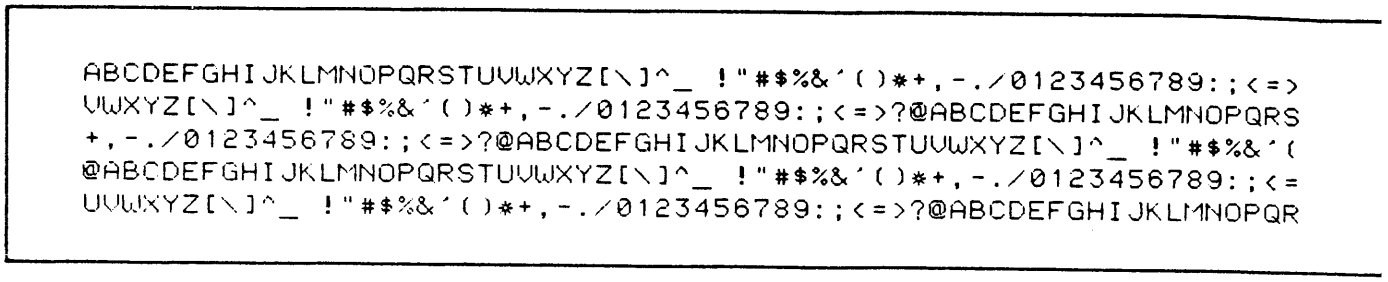


Figure A-7. 4695 Copier Test Pattern Hardcopy.

8259A PROGRAMMABLE INTERRUPT CONTROLLER SPECIFICATION

APPENDIX B

Appendix to IKON 10085 Interface Manual

Issued OCT 1984

8259A
PROGRAMMABLE INTERRUPT CONTROLLER

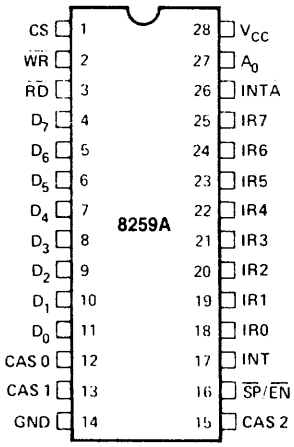
- MCS-86™ Compatible
- MCS-80/85™ Compatible
- Eight-Level Priority Controller
- Expandable to 64 Levels
- Programmable Interrupt Modes
- Individual Request Mask Capability
- Single +5V Supply (No Clocks)
- 28-Pin Dual-In-Line Package

The Intel® 8259A Programmable Interrupt Controller handles up to eight vectored priority interrupts for the CPU. It is cascadable for up to 64 vectored priority interrupts without additional circuitry. It is packaged in a 28-pin DIP, uses NMOS technology and requires a single +5V supply. Circuitry is static, requiring no clock input.

The 8259A is designed to minimize the software and real time overhead in handling multi-level priority interrupts. It has several modes, permitting optimization for a variety of system requirements.

The 8259A is fully upward compatible with the Intel® 8259. Software originally written for the 8259 will operate the 8259A in all 8259 equivalent modes (MCS-80/85, Non-Buffered, Edge Triggered).

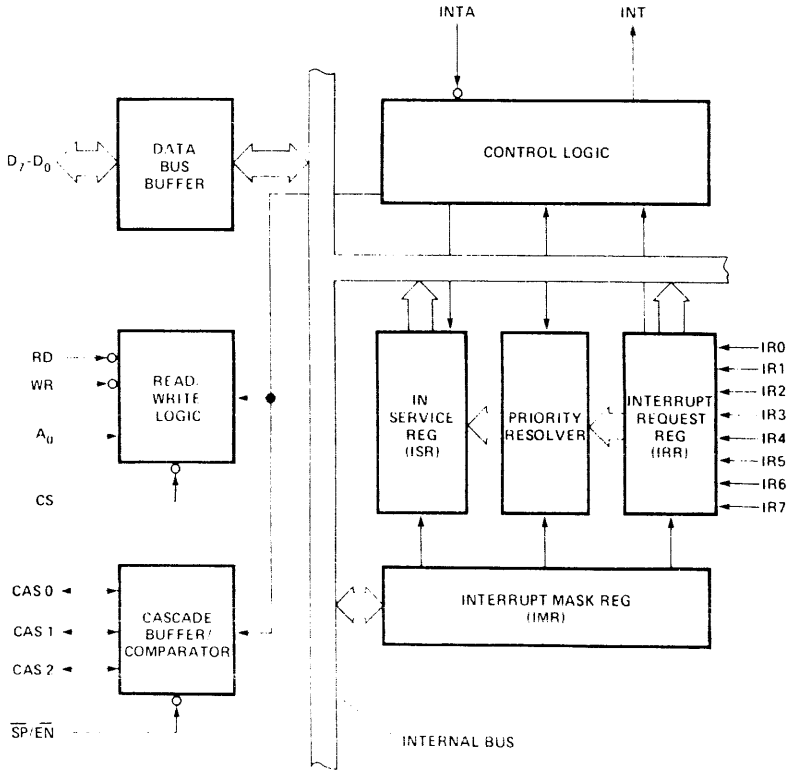
PIN CONFIGURATION



PIN NAMES

D_7-D_0	DATA BUS (BI DIRECTIONAL)
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A_0	COMMAND SELECT ADDRESS
$\overline{CS}$	CHIP SELECT
CAS2-CAS0	CASCADE LINES
$\overline{SP}/\overline{EN}$	SLAVE PROGRAM INPUT/ENABLE
INT	INTERRUPT OUTPUT
INTA	INTERRUPT ACKNOWLEDGE INPUT
IR0-IR7	INTERRUPT REQUEST INPUTS

BLOCK DIAGRAM



June 1978
9800665C

INTERRUPTS IN MICROCOMPUTER SYSTEMS

Microcomputer system design requires that I/O devices such as keyboards, displays, sensors and other components receive servicing in an efficient manner so that large amounts of the total system tasks can be assumed by the microcomputer with little or no effect on throughput.

The most common method of servicing such devices is the *Polled* approach. This is where the processor must test each device in sequence and in effect "ask" each one if it needs servicing. It is easy to see that a large portion of the main program is looping through this continuous polling cycle and that such a method would have a serious, detrimental effect on system throughput, thus limiting the tasks that could be assumed by the microcomputer and reducing the cost effectiveness of using such devices.

A more desirable method would be one that would allow the microprocessor to be executing its main program and only stop to service peripheral devices when it is told to do so by the device itself. In effect, the method would provide an external asynchronous input that would inform the processor that it should complete whatever instruction that is currently being executed and fetch a new routine that will service the requesting device. Once this servicing is complete, however, the processor would resume exactly where it left off.

This method is called *Interrupt*. It is easy to see that system throughput would drastically increase, and thus more tasks could be assumed by the microcomputer to further enhance its cost effectiveness.

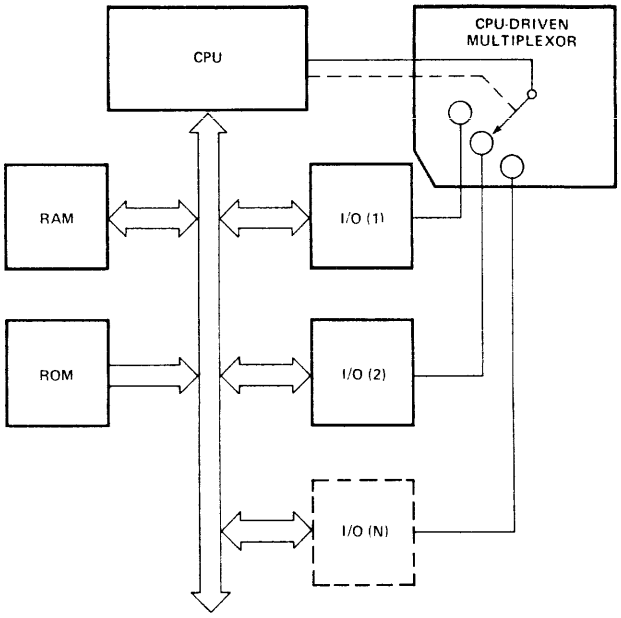
The Programmable Interrupt Controller (PIC) functions as an overall manager in an Interrupt-Driven system environment. It accepts requests from the peripheral equipment, determines which of the incoming requests is of the highest importance (priority), ascertains whether the incoming request has a higher priority value than the level currently being serviced, and issues an interrupt to the CPU based on this determination.

Each peripheral device or structure usually has a special program or "routine" that is associated with its specific functional or operational requirements; this is referred to as a "service routine". The PIC, after issuing an Interrupt to the CPU, must somehow input information into the CPU that can "point" the Program Counter to the service routine associated with the requesting device. This "pointer" is an address in a vectoring table and will often be referred to, in this document, as vectoring data.

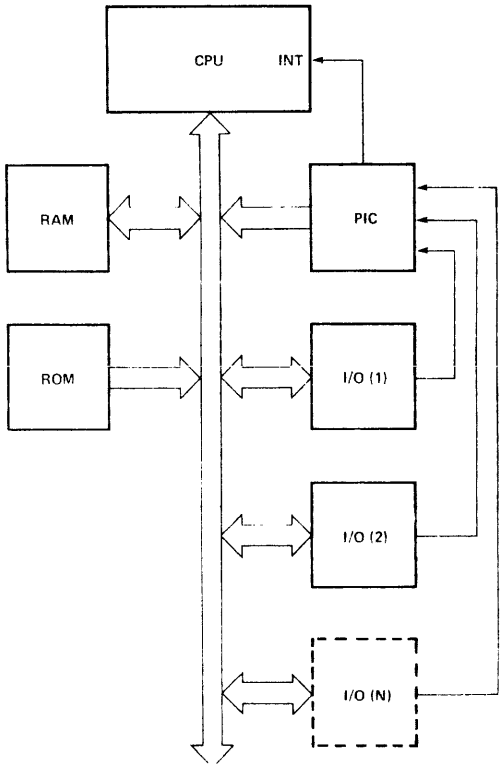
8259A BASIC FUNCTIONAL DESCRIPTION

GENERAL

The 8259A is a device specifically designed for use in real time, interrupt driven microcomputer systems. It manages eight levels or requests and has built-in features for expandability to other 8259A's (up to 64 levels). It is programmed by the system's software as an I/O peripheral. A selection of priority modes is available to the programmer so that the manner in which the requests are processed by the 8259A can be configured to match his system requirements. The priority modes can be changed or reconfigured dynamically at any time during the main program. This means that the complete interrupt structure can be defined as required, based on the total system environment.



Polled Method



Interrupt Method

INTERRUPT REQUEST REGISTER (IRR) AND IN-SERVICE REGISTER (ISR)

The interrupts at the IR input lines are handled by two registers in cascade, the Interrupt Request Register (IRR) and the In-Service Register (ISR). The IRR is used to store all the interrupt levels which are requesting service; and the ISR is used to store all the interrupt levels which are being serviced.

PRIORITY RESOLVER

This logic block determines the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during $\overline{INTA}$ pulse.

INTERRUPT MASK REGISTER (IMR)

The IMR stores the bits which mask the interrupt lines to be masked. The IMR operates on the IRR. Masking of a higher priority input will not affect the interrupt request lines of lower priority.

INT (INTERRUPT)

This output goes directly to the CPU interrupt input. The V_{OH} level on this line is designed to be fully compatible with the 8080A, 8085A and 8086 input levels.

$\overline{INTA}$ (INTERRUPT ACKNOWLEDGE)

$\overline{INTA}$ pulses will cause the 8259A to release vectoring information onto the data bus. The format of this data depends on the system mode (μPM) of the 8259A.

DATA BUS BUFFER

This 3-state, bidirectional 8-bit buffer is used to interface the 8259A to the system Data Bus. Control words and status information are transferred through the Data Bus Buffer.

READ/WRITE CONTROL LOGIC

The function of this block is to accept OUTput commands from the CPU. It contains the Initialization Command Word (ICW) registers and Operation Command Word (OCW) registers which store the various control formats for device operation. This function block also allows the status of the 8259A to be transferred onto the Data Bus.

$\overline{CS}$ (CHIP SELECT)

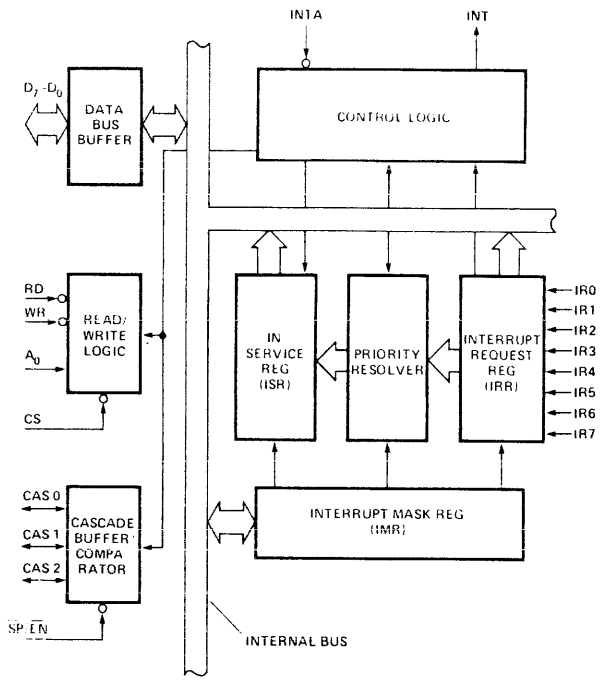
A LOW on this input enables the 8259A. No reading or writing of the chip will occur unless the device is selected.

$\overline{WR}$ (WRITE)

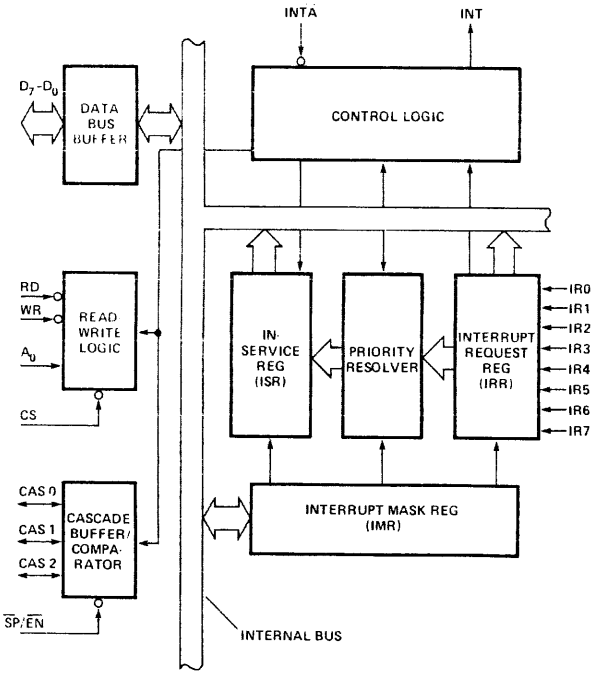
A LOW on this input enables the CPU to write control words (ICWs and OCWs) to the 8259A.

$\overline{RD}$ (READ)

A LOW on this input enables the 8259A to send the status of the Interrupt Request Register (IRR), In Service Register (ISR), the Interrupt Mask Register (IMR), or the Interrupt level onto the Data Bus.



8259A Block Diagram



8259A Block Diagram

A_0

This input signal is used in conjunction with $\overline{WR}$ and $\overline{RD}$ signals to write commands into the various command registers, as well as reading the various status registers of the chip. This line can be tied directly to one of the address lines.

THE CASCADE BUFFER/COMPARATOR

This function block stores and compares the IDs of all 8259A's used in the system. The associated three I/O pins (CAS0-2) are outputs when the 8259A is used as a master and are inputs when the 8259A is used as a slave. As a master, the 8259A sends the ID of the interrupting slave device onto the CAS0-2 lines. The slave thus selected will send its preprogrammed subroutine address onto the Data Bus during the next one or two consecutive $\overline{INTA}$ pulses. (See section "Cascading the 8259A".)

INTERRUPT SEQUENCE

The powerful features of the 8259A in a microcomputer system are its programmability and the interrupt routine addressing capability. The latter allows direct or indirect jumping to the specific interrupt routine requested without any polling of the interrupting devices. The normal sequence of events during an interrupt depends on the type of CPU being used.

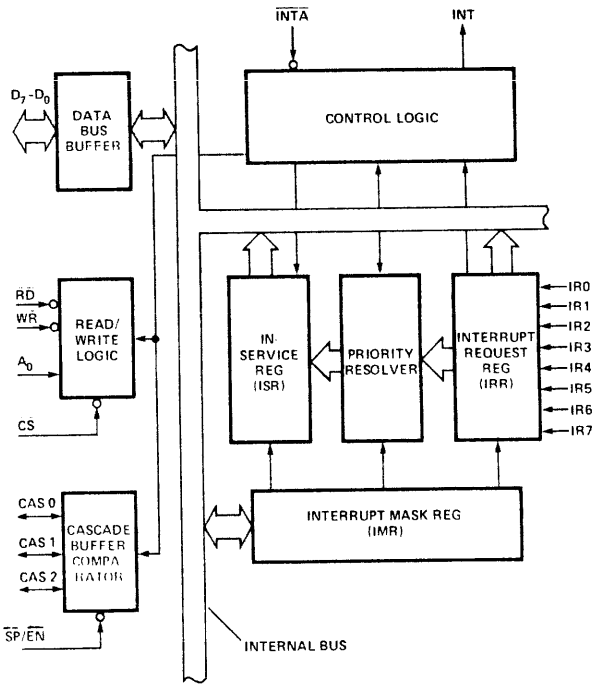
The events occur as follows in an MCS-80/85 system:

1. One or more of the INTERRUPT REQUEST lines (IR7-0) are raised high, setting the corresponding IRR bit(s).
2. The 8259A evaluates these requests, and sends an INT to the CPU, if appropriate.
3. The CPU acknowledges the INT and responds with an $\overline{INTA}$ pulse.
4. Upon receiving an $\overline{INTA}$ from the CPU group, the highest priority ISR bit is set, and the corresponding IRR bit is reset. The 8259A will also release a CALL instruction code (11001101) onto the 8-bit Data Bus through its D7-0 pins.
5. This CALL instruction will initiate two more $\overline{INTA}$ pulses to be sent to the 8259A from the CPU group.
6. These two $\overline{INTA}$ pulses allow the 8259A to release its preprogrammed subroutine address onto the Data Bus. The lower 8-bit address is released at the first $\overline{INTA}$ pulse and and the higher 8-bit address is released at the second $\overline{INTA}$ pulse.
7. This completes the 3-byte CALL instruction released by the 8259A. In the AEOI mode the ISR bit is reset at the end of the third $\overline{INTA}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt sequence.

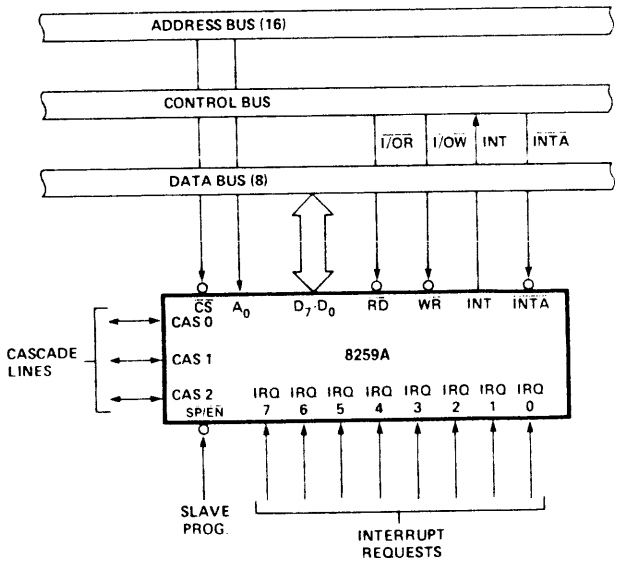
The events occurring in an MCS-86 system are the same until step 4.

4. Upon receiving an $\overline{INTA}$ from the CPU group, the highest priority ISR bit is set and the corresponding IRR bit is reset. The 8259A does not drive the Data Bus during this cycle.
5. The MCS-86 CPU will initiate a second $\overline{INTA}$ pulse. During this pulse, the 8259A releases an 8-bit pointer onto the Data Bus where it is read by the CPU.
6. This completes the interrupt cycle. In the AEOI mode the ISR bit is reset at the end of the second $\overline{INTA}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.

If no interrupt request is present at step 4 of either sequence (i.e., the request was too short in duration) the 8259A will issue an interrupt level 7. Both the vectoring bytes and the CAS lines will look like an interrupt level 7 was requested.



8259A Block Diagram



8259A Interface to Standard System Bus

INTERRUPT SEQUENCE OUTPUTS

MCS-80/85 SYSTEM

This sequence is timed by three $\overline{INTA}$ pulses. During the first $\overline{INTA}$ pulse the CALL opcode is enabled onto the data bus.

Content of First Interrupt Vector Byte

	D7	D6	D5	D4	D3	D2	D1	D0
CALL CODE	1	1	0	0	1	1	0	1

During the second $\overline{INTA}$ pulse the lower address of the appropriate service routine is enabled onto the data bus. When Interval = 4 bits A_5-A_7 are programmed, while A_0-A_4 are automatically inserted by the 8259A. When Interval = 8 only A_6 and A_7 are programmed, while A_0-A_5 are automatically inserted.

Content of Second Interrupt Vector Byte

IR	Interval = 4							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	A5	1	1	1	0	0
6	A7	A6	A5	1	1	0	0	0
5	A7	A6	A5	1	0	1	0	0
4	A7	A6	A5	1	0	0	0	0
3	A7	A6	A5	0	1	1	0	0
2	A7	A6	A5	0	1	0	0	0
1	A7	A6	A5	0	0	1	0	0
0	A7	A6	A5	0	0	0	0	0

IR	Interval = 8							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	1	1	1	0	0	0
6	A7	A6	1	1	0	0	0	0
5	A7	A6	1	0	1	0	0	0
4	A7	A6	1	0	0	0	0	0
3	A7	A6	0	1	1	0	0	0
2	A7	A6	0	1	0	0	0	0
1	A7	A6	0	0	1	0	0	0
0	A7	A6	0	0	0	0	0	0

During the third $\overline{INTA}$ pulse the higher address of the appropriate service routine, which was programmed as byte 2 of the initialization sequence (A_8-A_{15}), is enabled onto the bus.

Content of Third Interrupt Vector Byte

D7	D6	D5	D4	D3	D2	D1	D0
A15	A14	A13	A12	A11	A10	A9	A8

MCS-86 SYSTEM

MCS-86 mode is similar to MCS-80 mode except that only two Interrupt Acknowledge cycles are issued by the processor and no CALL opcode is sent to the processor. The first interrupt acknowledge cycle is similar to that of MCS-80/85 systems in that the 8259A uses it to internally freeze the state of the interrupts for priority resolution and as a master it issues the interrupt code on the cascade lines at the end of the $\overline{INTA}$ pulse. On this first cycle it does not issue any data to the processor and leaves its data bus buffers disabled. On the second interrupt acknowledge cycle in MCS-86 mode the master (or slave if so programmed) will send a byte of data to the processor with the acknowledged interrupt code composed as follows (note the state of the ADI mode control is ignored and A_5-A_{11} are unused in MCS-86 mode):

Content of Interrupt Vector Byte for MCS-86 System Mode

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	A15	A14	A13	A12	A11	1	1	1
IR6	A15	A14	A13	A12	A11	1	1	0
IR5	A15	A14	A13	A12	A11	1	0	1
IR4	A15	A14	A13	A12	A11	1	0	0
IR3	A15	A14	A13	A12	A11	0	1	1
IR2	A15	A14	A13	A12	A11	0	1	0
IR1	A15	A14	A13	A12	A11	0	0	1
IR0	A15	A14	A13	A12	A11	0	0	0

PROGRAMMING THE 8259A

The 8259A accepts two types of command words generated by the CPU:

1. *Initialization Command Words (ICWs):* Before normal operation can begin, each 8259A in the system must be brought to a starting point — by a sequence of 2 to 4 bytes timed by $\overline{WR}$ pulses. This sequence is described in Figure 1.

2. *Operation Command Words (OCWs):* These are the command words which command the 8259A to operate in various interrupt modes. These modes are:
   a. Fully nested mode
   b. Rotating priority mode
   c. Special mask mode
   d. Polled mode

The OCWs can be written into the 8259A anytime after initialization.

INITIALIZATION

GENERAL

Whenever a command is issued with A0 = 0 and D4 = 1, this is interpreted as Initialization Command Word 1 (ICW1). ICW1 starts the initialization sequence during which the following automatically occur.

a. The edge sense circuit is reset, which means that following initialization, an interrupt request (IR) input must make a low-to-high transition to generate an interrupt.
b. The Interrupt Mask Register is cleared.
c. IR 7 input is assigned priority 7.
d. The slave mode address is set to 7.
e. Special Mask Mode is cleared and Status Read is set to IRR.
f. If IC4 = 0, then all functions selected in ICW4 are set to zero. (Non-Buffered mode*, no Auto-EOI, MCS-80/85 system).

***Note:** Master/Slave in ICW4 is only used in the buffered mode.

A_0	D_4	D_3	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	INPUT OPERATION (READ)
0			0	1	0	IRR, ISR or Interrupting Level → DATA BUS (Note 1)
1			0	1	0	IMR → DATA BUS
						OUTPUT OPERATION (WRITE)
0	0	0	1	0	0	DATA BUS → OCW2
0	0	1	1	0	0	DATA BUS → OCW3
0	1	X	1	0	0	DATA BUS → ICW1
1	X	X	1	0	0	DATA BUS → OCW1, ICW2, ICW3, ICW4 (Note 2)
						DISABLE FUNCTION
X	X	X	1	1	0	DATA BUS → 3-STATE
X	X	X	X	X	1	DATA BUS → 3-STATE

Notes: 1. Selection of IRR, ISR or Interrupting Level is based on the content of OCW3 written before the READ operation.
2. On-chip sequencer logic queues these commands into proper sequence.

8259A Basic Operation

INITIALIZATION COMMAND WORDS 1 AND 2 (ICW1, ICW2)

A_5-A_{15}: *Page starting address of service routines.* In an MCS 80/85 system, the 8 request levels will generate CALLs to 8 locations equally spaced in memory. These can be programmed to be spaced at intervals of 4 or 8 memory locations, thus the 8 routines will occupy a page of 32 or 64 bytes, respectively.

The address format is 2 bytes long (A_0-A_{15}). When the routine interval is 4, A_0-A_4 are automatically inserted by the 8259A, while A_5-A_{15} are programmed externally. When the routine interval is 8, A_0-A_5 are automatically inserted by the 8259A, while A_6-A_{15} are programmed externally.

The 8-byte interval will maintain compatibility with current software, while the 4-byte interval is best for a compact jump table.

In an MCS-86 system A_{15}-A_{11} are inserted in the five most significant bits of the vectoring byte and the 8259A sets the three least significant bits according to the interrupt level. A_{10}-A_5 are ignored and ADI (Address interval) has no effect.

LTIM: If LTIM = 1, then the 8259A will operate in the level interrupt mode. Edge detect logic on the interrupt inputs will be disabled.

ADI: CALL address interval. ADI = 1 then interval = 4; ADI = 0 then interval = 8.

SNGL: Single. Means that this is the only 8259A in the system. If SNGL = 1 no ICW3 will be issued.

IC4: If this bit is set — ICW4 has to be read. If ICW4 is not needed, set IC4 = 0.

INITIALIZATION COMMAND WORD 3 (ICW3)

This word is read only when there is more than one 8259A in the system and cascading is used, in which case SNGL = 0. It will load the 8-bit slave register. The functions of this register are:

a. In the master mode (either when $\overline{SP}$ = 1, or in buffered mode when M/S = 1 in ICW4) a "1" is set for each slave in the system. The master then will release byte 1 of the call sequence (for MCS-80/85 system) and will enable the corresponding slave to release bytes 2 and 3 (for MCS-86 only byte 2) through the cascade lines.

b. In the slave mode (either when $\overline{SP}$ = 0, or if BUF = 1 and M/S = 0 in ICW4) bits 2-0 identify the slave. The slave compares its cascade input with these bits and, if they are equal, bytes 2 and 3 of the call sequence (or just byte 2 for MCS-86) are released by it on the Data Bus.

INITIALIZATION COMMAND WORD 4 (ICW4)

FNM: If FNM = 1 the fully nested mode is programmed.

BUF: If BUF = 1 the buffered mode is programmed. In buffered mode $\overline{SP}/\overline{EN}$ becomes an enable output and the master/slave determination is by M/S.

M/S: If buffered mode is selected: M/S = 1 means the 8259A is programmed to be a master, M/S = 0 means the 8259A is programmed to be a slave. If BUF = 0, M/S has no function.

AEOI: If AEOI = 1 the automatic end of interrupt mode is programmed.

μPM: Microprocessor mode: μPM = 0 sets the 8259A for MCS-80/85 system operation, μPM = 1 sets the 8259A for MCS-86 system operation.

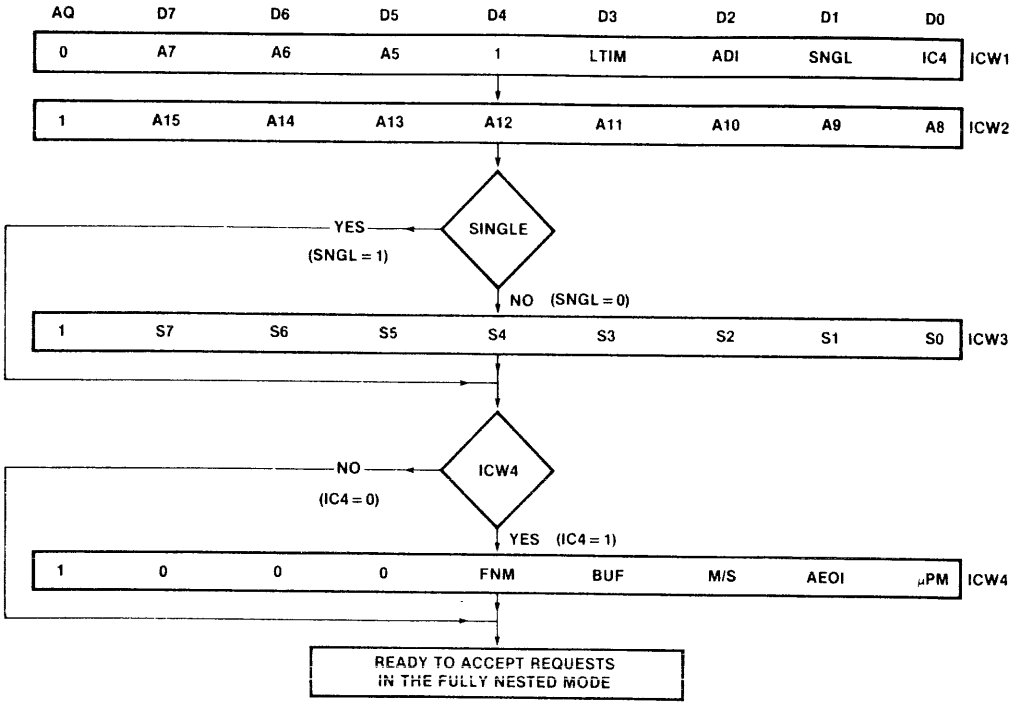
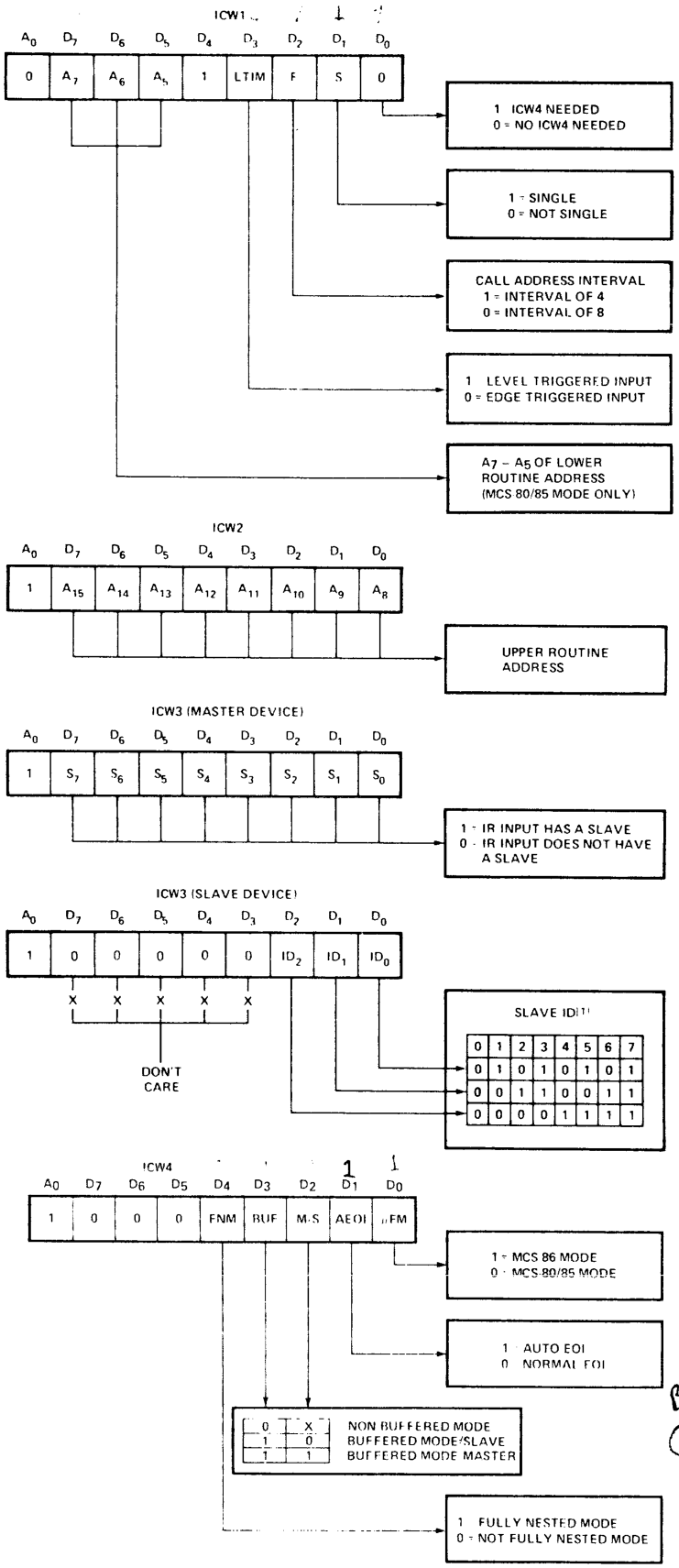


Figure 1. Initialization Sequence



NOTE 1: SLAVED ID IS EQUAL TO THE CORRESPONDING MASTER IR INPUT.
NOTE 2: X INDICATED "DON'T CARE".

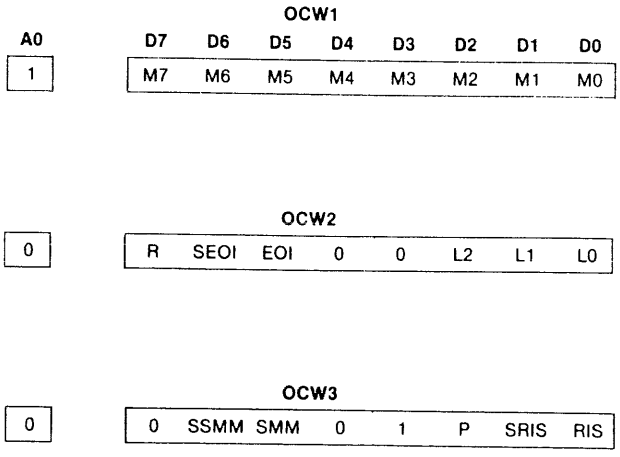
But not when single = ϕ
(master-slave!!)

Initialization Command Word Format

OPERATION COMMAND WORDS (OCWs)

After the Initialization Command Words (ICWs) are programmed into the 8259A, the chip is ready to accept interrupt requests at its input lines. However, during the 8259A operation, a selection of algorithms can command the 8259A to operate in various modes through the Operation Command Words (OCWs).

OPERATION CONTROL WORDS (OCWs)



OPERATION CONTROL WORD 1 (OCW1)

OCW1 sets and clears the mask bits in the Interrupt Mask Register (IMR). M_7-M_0 represent the eight mask bits. M = 1 indicates the channel is masked (inhibited). M = 0 indicates the channel is enabled.

OPERATION CONTROL WORD 2 (OCW2)

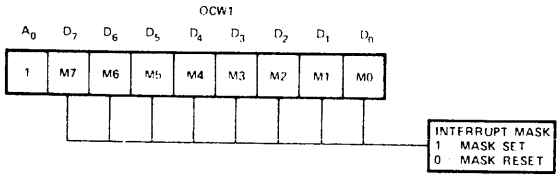
R, SEOI, EOI — These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations can be found on the Operation Command Word Format.

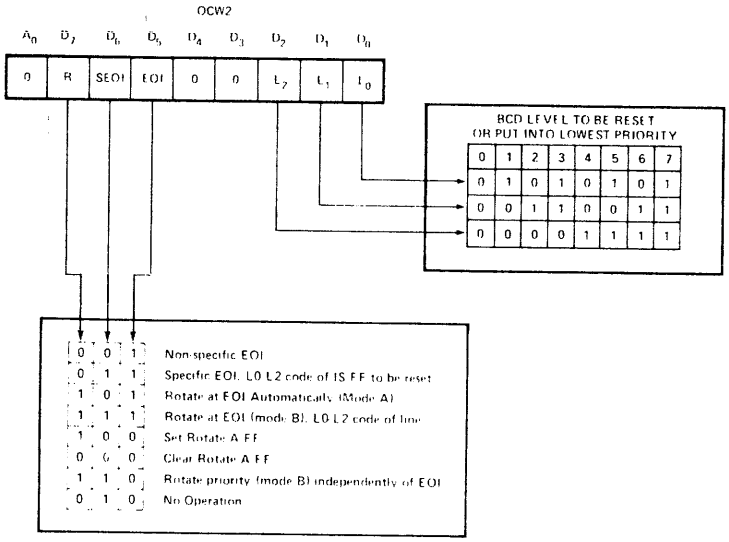
L_2, L_1, L_0 — These bits determine the interrupt level acted upon when the SEOI bit is active.

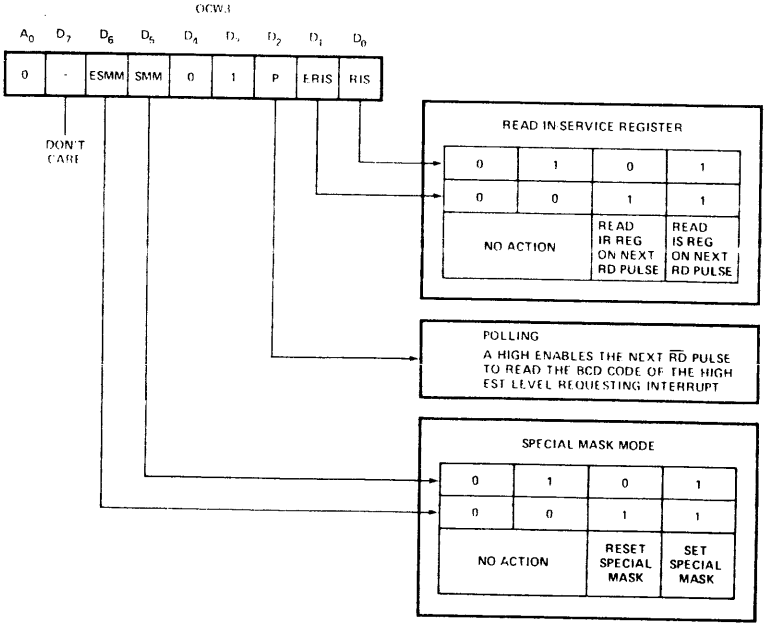
OPERATION CONTROL WORD 3 (OCW3)

ESMM — Enable Special Mask Mode. When this bit is set to 1 it enables the SMM bit to set or reset the Special Mask Mode. When ESMM = 0 the SMM bit becomes a "don't care".

SMM — Special Mask Mode. If ESMM = 1 and SMM = 1 the 8259A will enter Special Mask Mode. If ESMM = 1 and SMM = 0 the 8259A will revert to normal mask mode. When ESMM = 0, SMM has no effect.







Operation Command Word Format

INTERRUPT MASKS

Each Interrupt Request input can be masked individually by the Interrupt Mask Register (IMR) programmed through OCW1. Each bit in the IMR masks one interrupt channel if it is set (1). Bit 0 masks IR0, Bit 1 masks IR1 and so forth. Masking an IR channel does not affect the other channels operation.

SPECIAL MASK MODE

Some applications may require an interrupt service routine to dynamically alter the system priority structure during its execution under software control. For example, the routine may wish to inhibit lower priority requests for a portion of its execution but enable some of them for another portion.

The difficulty here is that if an Interrupt Request is acknowledged and an End of Interrupt command did not reset its IS bit (i.e., while executing a service routine), the 8259A would have inhibited all lower priority requests with no easy way for the routine to enable them

That is where the Special Mask Mode comes in. In the special Mask Mode, when a mask bit is set in OCW1, it inhibits further interrupts at that level *and enables* interrupts from *all other* levels (lower as well as higher) that are not masked.

Thus, any interrupts may be selectively enabled by loading the mask register.

The special Mask Mode is set by OCW3 where: SSMM = 1, SMM = 1, and cleared where SSMM = 1, SMM = 0.

BUFFERED MODE

When the 8259A is used in a large system where bus driving buffers are required on the data bus and the cascading mode is used, there exists the problem of enabling buffers.

The buffered mode will structure the 8259A to send an enable signal on $\overline{SP}/\overline{EN}$ to enable the buffers. In this mode, whenever the 8259A's data bus outputs are enabled, the $\overline{SP}/\overline{EN}$ output becomes active.

This modification forces the use of software programming to determine whether the 8259A is a master or a slave. Bit 3 in ICW4 programs the buffered mode, and bit 2 in ICW4 determines whether it is a master or a slave.

NESTED MODE

This mode is entered after initialization unless another mode is programmed. The interrupt requests are ordered in priority from 0 through 7 (0 highest). When an interrupt is acknowledged the highest priority request is determined and its vector placed on the bus. Additionally, a bit of the Interrupt Service register (IS0-7) is set. This bit remains set until the microprocessor issues an

End of Interrupt (EOI) command immediately before returning from the service routine, or if AEOI (Automatic End of Interrupt) bit is set, until the trailing edge of the last $\overline{INTA}$. While the IS bit is set, all further interrupts of the same or lower priority are inhibited, while higher levels will generate an interrupt (which will be acknowledged only if the microprocessor internal Interrupt enable flip-flop has been re-enabled through software).

After the initialization sequence, IR0 has the highest priority and IR7 the lowest. Priorities can be changed, as will be explained, in the rotating priority mode.

THE SPECIAL FULLY NESTED MODE

This mode will be used in the case of a big system where cascading is used, and the priority has to be conserved within each slave. In this case the fully nested mode will be programmed to the master (using ICW4). This mode is similar to the normal nested mode with the following exceptions:

a. When an interrupt request from a certain slave is in service this slave is not locked out from the master's priority logic and further interrupt requests from higher priority IR's within the slave will be recognized by the master and will initiate interrupts to the processor. (In the normal nested mode a slave is masked out when its request is in service and no higher requests from the same slave can be serviced.)

b. When exiting the Interrupt Service routine the software has to check whether the interrupt serviced was the only one from that slave. This is done by sending a non-specific End of Interrupt (EOI) command to the slave and then reading its In-Service register and checking for zero. If it is empty, a non-specific EOI can be sent to the master too. If not, no EOI should be sent.

POLL

In this mode the microprocessor internal Interrupt Enable flip-flop is reset, disabling its interrupt input. Service to devices is achieved by programmer initiative using a Poll command.

The Poll command is issued by setting P = "1" in OCW3. The 8259A treats the next $\overline{RD}$ pulse to the 8259A (i.e., $\overline{RD} = 0$, $\overline{CS} = 0$) as an interrupt acknowledge, sets the appropriate IS bit if there is a request, and reads the priority level. Interrupt is frozen from $\overline{WR}$ to $\overline{RD}$.

The word enabled onto the data bus during $\overline{RD}$ is:

D7	D6	D5	D4	D3	D2	D1	D0
I	—	—	—	—	W2	W1	W0

W0-W2: Binary code of the highest priority level requesting service.

I: Equal to a "1" if there is an interrupt.

This mode is useful if there is a routine command common to several levels so that the $\overline{INTA}$ sequence is not needed (saves ROM space). Another application is to use the poll mode to expand the number of priority levels to more than 64.

END OF INTERRUPT (EOI)

The In Service (IS) bit can be reset either automatically following the trailing edge of the last in sequence $\overline{INTA}$ pulse (when AEOI bit in ICW1 is set) or by a command word that must be issued to the 8259A before returning from a service routine (EOI command). An EOI command must be issued twice, once for the master and once for the corresponding slave if slaves are in use.

There are two forms of EOI command: Specific and Non-Specific. When the 8259A is operated in modes which preserve the fully nested structure, it can determine which IS bit to reset on EOI. When a Non-Specific EOI command is issued the 8259A will automatically reset the highest IS bit of those that are set, since in the nested mode the highest IS level was necessarily the last level acknowledged and serviced.

However, when a mode is used which may disturb the fully nested structure, the 8259A may no longer be able to determine the last level acknowledged. In this case a Specific End of Interrupt (SEOI) must be issued which includes as part of the command the IS level to be reset. EOI is issued whenever E = 1, in OCW2, where L0-L2 is the binary level of the IS bit to be reset. Note that although the Rotate command can be issued together with an EOI where E = 1, it is not necessarily tied to it.

It should be noted that an IS bit that is masked by an IMR bit will not be cleared by a non-specific EOI if the 8259A is in the Special Mask Mode.

AUTOMATIC END OF INTERRUPT (AEOI) MODE

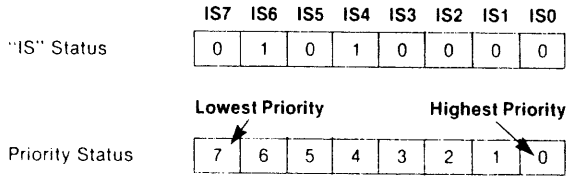
If AEOI = 1 in ICW4, then the 8259A will operate in AEOI mode continuously until reprogrammed by ICW4. In this mode the 8259A will automatically perform a non-specific EOI operation at the trailing edge of the last interrupt acknowledge pulse (third pulse in MCS-80/85, second in MCS-86). Note that from a system standpoint, this mode should be used only when a nested multilevel interrupt structure is not required within a single 8259A.

To achieve automatic rotation (Rotate Mode A) within AEOI, there is a special rotate flip-flop. It is set by OCW2 with R = 1, SEOI = *0*, E = 0, and cleared with R = 0, SEOI = 0, E = 0.

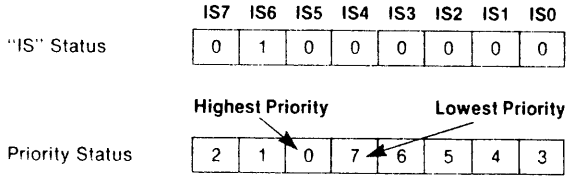
ROTATING PRIORITY MODE A (AUTOMATIC ROTATION) FOR EQUAL PRIORITY DEVICES

In some applications there are a number of interrupting devices of equal priority. In this mode a device, after being serviced, receives the lowest priority, so a device requesting an interrupt will have to wait, in the worst case until each of 7 other devices are serviced at most *once*. For example, if the priority and "in service" status is:

Before Rotate (IR4 the highest priority requiring service)



After Rotate (IR4 was serviced, all other priorities rotated correspondingly)



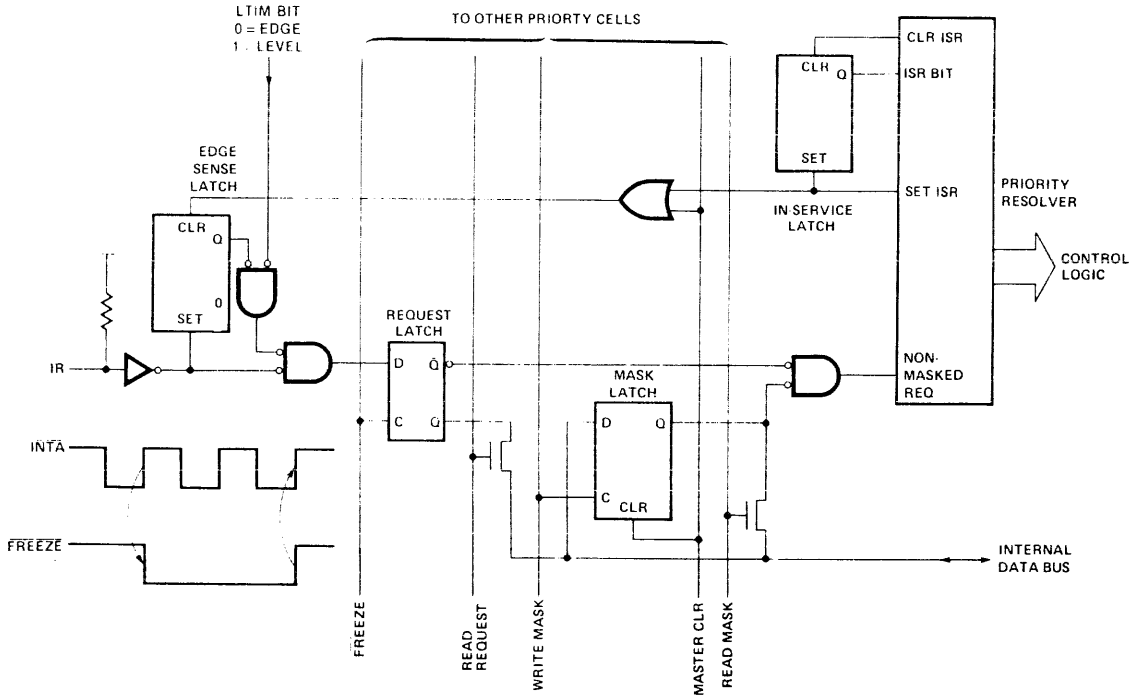
The Rotate command mode A is issued in OCW2 where: R = 1, E = 1, SEOI = 0. Internal status is updated by an End of Interrupt (EOI or AEOI) command. If R = 1, E = 0, SEOI = 0, a "Rotate-A" flip-flop is set. This is useful in AEOI, and described under Automatic End of Interrupt.

ROTATING PRIORITY MODE B (ROTATION BY SOFTWARE)

The programmer can change priorities by programming the bottom priority and thus fixing all other priorities; i.e., if IR5 is programmed as the bottom priority device, then IR6 will have the highest one.

The Rotate command is issued in OCW2 where: R = 1, SEOI = 1; L0-L2 is the binary priority level code of the bottom priority device.

Observe that in this mode internal status is updated by software control during OCW2. However, it is independent of the End of Interrupt (EOI) command (also executed by OCW2). Priority changes can be executed during an EOI command or independently.



NOTES

1. MASTER CLEAR ACTIVE ONLY DURING ICW1
2. FREEZE/ IS ACTIVE DURING $\overline{\text{INTA}}$/ AND POLL SEQUENCES ONLY
3. TRUTH TABLE FOR D-LATCH

C	D	Q	OPERATION
1	Di	Di	FOLLOW
0	X	Qn-1	HOLD

Priority Cell

LEVEL TRIGGERED MODE

This mode is programmed using bit 3 in ICW1.

If LTM = '1', an interrupt request will be recognized by a 'high' level on IR Input, and there is no need for an edge detection. The interrupt request must be removed before the EOI command is issued or the CPU interrupt is enabled to prevent a second interrupt from occurring.

The above figure shows a conceptual circuit to give the reader an understanding of the level sensitive and edge sensitive input circuitry of the 8259A. Be sure to note that the request latch is a transparent D type latch.

READING THE 8259A STATUS

The input status of several internal registers can be read to update the user information on the system. The following registers can be read by issuing a suitable OCW3 and reading with $\overline{\text{RD}}$.

Interrupt Mask Register: 8-bit register whose content specifies the interrupt request lines being masked. acknowledged. The highest request level is reset from the IRR when an interrupt is acknowledged. (Not affected by IMR.)

In-Service Register (ISR): 8-bit register which contains the priority levels that are being serviced. The ISR is updated when an End of Interrupt command is issued.

Interrupt Mask Register: 8-bit register which contains the interrupt request lines which are masked.

The IRR can be read when, prior to the $\overline{\text{RD}}$ pulse, a $\overline{\text{WR}}$ pulse is issued with OCW3 (ERIS = 1, RIS = 0.)

The ISR can be read in a similar mode when ERIS = 1, RIS = 1 in the OCW3.

There is no need to write an OCW3 before every status read operation, as long as the status read corresponds with the previous one; i.e., the 8259A "remembers" whether the IRR or ISR has been previously selected by the OCW3.

After initialization the 8259A is set to IRR.

For reading the IMR, no OCW3 is needed. The output data bus will contain the IMR whenever $\overline{\text{RD}}$ is active and A0 = 1.

Polling overrides status read when P = 1, ERIS = 1 in OCW3.

SUMMARY OF 8259A INSTRUCTION SET

Inst. #	Mnemonic		A0	D7	D6	D5	D4	D3	D2	D1	D0	Operation Description
1	ICW1	A	0	A7	A6	A5	1	0	1	1	0	Format = 4, single, edge triggered
2	ICW1	B	0	A7	A6	A5	1	1	1	1	0	Format = 4, single, level triggered
3	ICW1	C	0	A7	A6	A5	1	0	1	0	0	Byte 1 Initialization — Format = 4, not single, edge triggered
4	ICW1	D	0	A7	A6	A5	1	1	1	0	0	Format = 4, not single, level triggered
5	ICW1	E	0	A7	A6	0	1	0	0	1	0	No ICW4 Required — Format = 8, single, edge triggered
6	ICW1	F	0	A7	A6	0	1	1	0	1	0	Format = 8, single, level triggered
7	ICW1	G	0	A7	A6	0	1	0	0	0	0	Format = 8, not single, edge triggered
8	ICW1	H	0	A7	A6	0	1	1	0	0	0	Format = 8, not single, level triggered
9	ICW1	I	0	A7	A6	A5	1	0	1	1	1	Format = 4, single, edge triggered
10	ICW1	J	0	A7	A6	A5	1	1	1	1	1	Format = 4, single, level triggered
11	ICW1	K	0	A7	A6	A5	1	0	1	0	1	Byte 1 Initialization — Format = 4, not single, edge triggered
12	ICW1	L	0	A7	A6	A5	1	1	1	0	1	Format = 4, not single, level triggered
13	ICW1	M	0	A7	A6	0	1	0	0	1	1	ICW4 Required — Format = 8, single, edge triggered
14	ICW1	N	0	A7	A6	0	1	1	0	1	1	Format = 8, single, level triggered
15	ICW1	O	0	A7	A6	0	1	0	0	0	1	Format = 8, not single, edge triggered
16	ICW1	P	0	A7	A6	0	1	1	0	0	1	Format = 8, not single, level triggered
17	ICW2		1	A15	A14	A13	A12	A11	A10	A9	A8	Byte 2 initialization
18	ICW3	M	1	S7	S6	S5	S4	S3	S2	S1	S0	Byte 3 initialization — master
19	ICW3	S	1	0	0	0	0	0	S2	S1	S0	Byte 3 initialization — slave
20	ICW4	A	1	0	0	0	0	0	0	0	0	No action, redundant
21	ICW4	B	1	0	0	0	0	0	0	0	1	Non-buffered mode, no AEOI, MCS-86
22	ICW4	C	1	0	0	0	0	0	0	1	0	Non-buffered mode, AEOI, MCS-80/85
23	ICW4	D	1	0	0	0	0	0	0	1	1	Non-buffered mode, AEOI, MCS-86
24	ICW4	E	1	0	0	0	0	0	1	0	0	No action, redundant
25	ICW4	F	1	0	0	0	0	0	1	0	1	Non-buffered mode, no AEOI, MCS-86
26	ICW4	G	1	0	0	0	0	0	1	1	0	Non-buffered mode, AEOI, MCS-80/85
27	ICW4	H	1	0	0	0	0	0	1	1	1	Non-buffered mode, AEOI, MCS-86
28	ICW4	I	1	0	0	0	0	1	0	0	0	Buffered mode, slave, no AEOI, MCS-80/85
29	ICW4	J	1	0	0	0	0	1	0	0	1	Buffered mode, slave, no AEOI, MCS-86
30	ICW4	K	1	0	0	0	0	1	0	1	0	Buffered mode, slave, AEOI, MCS-80/85
31	ICW4	L	1	0	0	0	0	1	0	1	1	Buffered mode, slave, AEOI, MCS-86
32	ICW4	M	1	0	0	0	0	1	1	0	0	Buffered mode, master, no AEOI, MCS-80/85
33	ICW4	N	1	0	0	0	0	1	1	0	1	Buffered mode, master, no AEOI, MCS-86
34	ICW4	O	1	0	0	0	0	1	1	1	0	Buffered mode, master, AEOI, MCS-80/85
35	ICW4	P	1	0	0	0	0	1	1	1	1	Buffered mode, master, AEOI, MCS-86
36	ICW4	NA	1	0	0	0	1	0	0	0	0	Fully nested mode, MCS-80, non-buffered, no AEOI
37	ICW4	NB	1	0	0	0	1	0	0	0	1	ICW4 NB through ICW4 ND are identical to ICW4 B through ICW4 D with the addition of Fully Nested Mode
38	ICW4	NC	1	0	0	0	1	0	0	1	0	
39	ICW4	ND	1	0	0	0	1	0	0	1	1	
40	ICW4	NE	1	0	0	0	1	0	1	0	0	Fully Nested Mode, MCS-80/85, non-buffered, no AEOI
41	ICW4	NF	1	0	0	0	1	0	1	0	1	ICW4 NF through ICW4 NP are identical to ICW4 F through ICW4 P with the addition of Fully Nested Mode
42	ICW4	NG	1	0	0	0	1	0	1	1	0	
43	ICW4	NH	1	0	0	0	1	0	1	1	1	
44	ICW4	NI	1	0	0	0	1	1	0	0	0	
45	ICW4	NJ	1	0	0	0	1	1	0	0	1	
46	ICW4	NK	1	0	0	0	1	1	0	1	0	
47	ICW4	NL	1	0	0	0	1	1	0	1	1	
48	ICW4	NM	1	0	0	0	1	1	1	0	0	
49	ICW4	NN	1	0	0	0	1	1	1	0	1	
50	ICW4	NO	1	0	0	0	1	1	1	1	0	
51	ICW4	NP	1	0	0	0	1	1	1	1	1	
36	OCW1		1	M7	M6	M5	M4	M3	M2	M1	M0	Load mask register, read mask register
37	OCW2	E	0	0	0	1	0	0	0	0	0	Non-specific EOI
38	OCW2	SE	0	0	1	1	0	0	L2	L1	L0	Specific EOI. L0-L2 code of IS FF to be reset
39	OCW2	RE	0	1	0	1	0	0	0	0	0	Rotate at EOI Automatically (Mode A)
40	OCW2	RSE	0	1	1	1	0	0	L2	L1	L0	Rotate at EOI (mode B). L0-L2 code of line
41	OCW2	R	0	1	0	0	0	0	0	0	0	Set Rotate A FF
42	OCW2	CR	0	0	0	0	0	0	0	0	0	Clear Rotate A FF
43	OCW2	RS	0	1	1	0	0	0	L2	L1	L0	Rotate priority (mode B) independently of EOI
44	OCW3	P	0	0	0	0	0	1	1	0	0	Poll mode
45	OCW3	RIS	0	0	0	0	0	1	0	1	1	Read IS register

SUMMARY OF 8259A INSTRUCTION SET (Cont.)

Inst. #	Mnemonic	A0	D7	D6	D5	D4	D3	D2	D1	D0	Operation Description
46	OCW3 RR	0	0	0	0	0	1	0	1	0	Read request register
47	OCW3 SM	0	0	1	1	0	1	0	0	0	Set special mask mode
48	OCW3 RSM	0	0	1	0	0	1	0	0	0	Reset special mask mode

Note: 1. In the master mode SP pin = 1, in slave mode SP = 0

Cascading

The 8259A can be easily interconnected in a system of one master with up to eight slaves to handle up to 64 priority levels.

A typical MCS-80/85 system is shown in Figure 2. The master controls, through the 3 line cascade bus, which one of the slaves will release the corresponding address.

As shown in Figure 2, the slave interrupt outputs are connected to the master interrupt request inputs. When a slave request line is activated and afterwards acknowledged, the master will enable the corresponding slave to release the device routine address during bytes 2 and 3 of $\overline{INTA}$. (Byte 2 only for MCS-86).

The cascade bus lines are normally low and will contain the slave address code from the trailing edge of the first $\overline{INTA}$ pulse to the trailing edge of the third pulse. It is obvious that each 8259A in the system must follow a separate initialization sequence and can be programmed to work in a different mode. An EOI command must be issued twice: once for the master and once for the corresponding slave. An address decoder is required to activate the Chip Select ($\overline{CS}$) input of each 8259A.

The cascade lines of the Master 8259A are activated for any interrupt input, even if no slave is connected to that input.

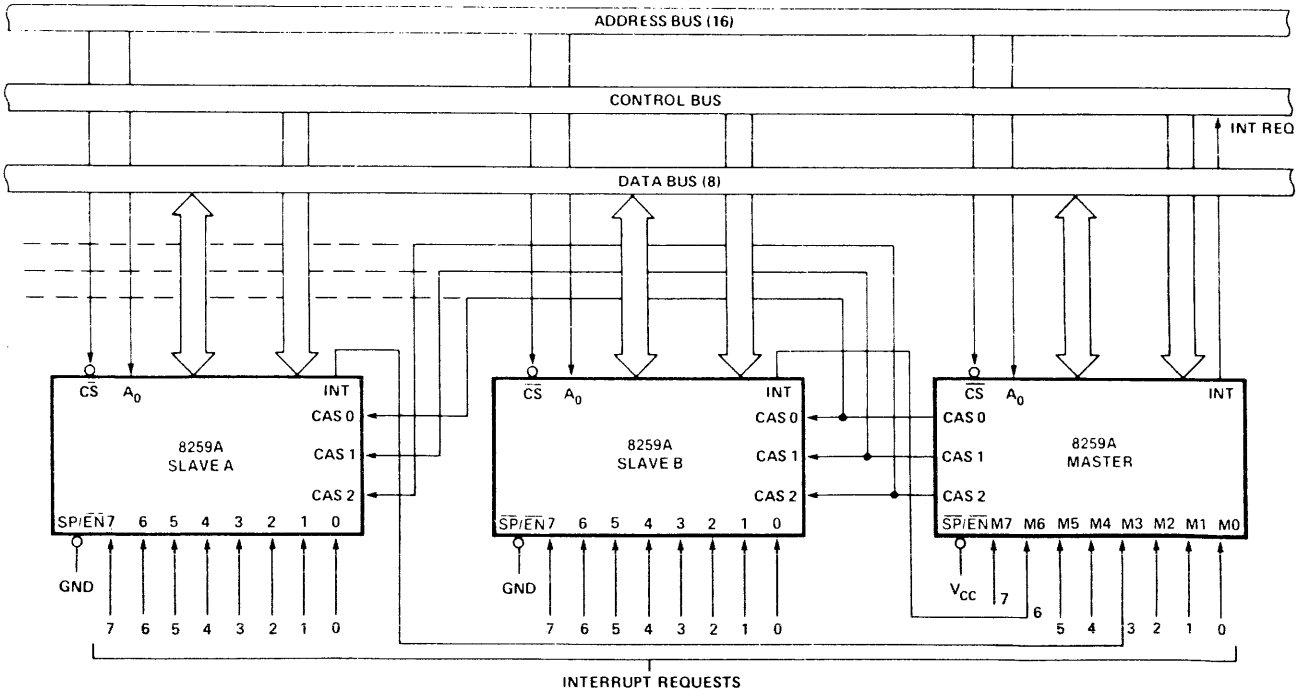


Figure 2. Cascading the 8259A

PIN FUNCTIONS

Name	I/O	Pin #	Function
V_{CC}		28	+5V supply.
GND		14	Ground.
D_{0-7}	I/O	11-4	Bidirectional data bus, used for: a) programming the mode of the 8259A (programming is done by software); b) the microprocessor can read the status of the 8259A; c) the 8259A will send vectoring data to the microprocessor when an interrupt is acknowledged.
IR_{0-7}	I	18-25	Interrupt Requests: These are asynchronous inputs. A positive-going edge will generate an interrupt request. Thus a request can be generated by raising the line and holding it high until acknowledged, or by a negative pulse. In level triggered mode, no edge is required. These lines are active HIGH.
$\overline{RD}$	I	3	Read (generally from 8228 in MCS-80 system or from 8086 in MCS-86 system).
$\overline{WR}$	I	2	Write (generally from 8228 in MCS-80 sytem or from 8086 in MCS-86 system).
$\overline{INTA}$	I	26	Interrupt Acknowledge (generally from 8228 in MCS-80 system, 8086 in MCS-86 system). The 8288 generates three distinct $\overline{INTA}$ pulses when a CALL is inserted, the 8086 produces two distinct $\overline{INTA}$ pulses during an interrupt cycle.
$\overline{CS}$	I	1	Chip Select: $\overline{RD}$ and $\overline{WR}$ are enabled by Chip Select, whereas Interrupt Acknowledge is independent of Chip Select.
A0	I	27	Usually the least significant bit of the microprocessor address output. When A0 = 1 the Interrupt Mask Register can be loaded or read. When A0 = 0 the 8259A mode can be programmed or its status can be read. $\overline{CS}$ is active LOW.
INT	O	17	Goes directly to the microprocessor interrrupt input. This output will have high V_{OH} to match the 8080 3.3V V_{IH}. INT is active HIGH.
C0-C2	I/O	12 13 15	Three cascade lines, outputs in master mode and inputs in slave mode. The master issues the binary code of the acknowledged interrupt level on these lines. Each slave compares this code with its own.
$\overline{SP}/\overline{EN}$	I/O	16	$\overline{SP}/\overline{EN}$ is a dual function pin. In the buffered mode $\overline{SP}/\overline{EN}$ is used to enable bus transceivers ($\overline{EN}$). In the non-buffered mode $\overline{SP}/\overline{EN}$ determines if this 8259A is a master or a slave. If $\overline{SP}$ = 1 the 8259A is master; $\overline{SP}$ = 0 indicates a slave.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... −40°C to 85°C
Storage Temperature ..... −65°C to +150°C
Voltage On Any Pin
With Respect to Ground ..... −0.5V to +7V
Power Dissipation ..... 1 Watt

COMMENT
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS

T_A = 0°C to 70°C V_{CC} = 5V ± 5% (8259A-8) V_{CC} = 5V ± 10% (8259A)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	−.5	.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + .5V	V	
V_{OL}	Output Low Voltage		.45	V	I_{OL} = 2.2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 μA
$V_{OH(INT)}$	Interrupt Output High Voltage	3.5 2.4		V V	I_{OH} = −100 μA I_{OH} = −400 μA
I_{LI}	Input Load Current		10	μA	V_{IN} = V_{CC} to 0V
I_{LOL}	Output Leakage Current		−10	μA	V_{OUT} = 0.45V
I_{LOH}	Output Leakage Current		10	μA	V_{OUT} = V_{CC}
I_{CC}	V_{CC} Supply Current		85	mA	

8259A A.C. CHARACTERISTICS

$T_A = 0°C$ to $70°C$ $V_{CC} = 5V \pm 5\%$ (8259A-8) $V_{CC} = 5V \pm 10\%$ (8259A)

TIMING REQUIREMENTS

Symbol	Parameter	8259A-8 Min.	8259A-8 Max.	8259A Min.	8259A Max.	Units	Test Conditions
TAHRL	A0/$\overline{CS}$ Setup to $\overline{RD}$/$\overline{INTA}$↓	50		0		ns	
TRHAX	A0/$\overline{CS}$ Hold after $\overline{RD}$/$\overline{INTA}$↑	5		0		ns	
TRLRH	$\overline{RD}$ Pulse Width	420		235		ns	
TAHWL	A0/$\overline{CS}$ Setup to$\overline{WR}$↓	50		0		ns	
TWHAX	A0/$\overline{CS}$ Hold after $\overline{WR}$↑	20		0		ns	
TWLWH	$\overline{WR}$ Pulse Width	400		290		ns	
TDVWH	Data Setup to $\overline{WR}$↑	300		240		ns	
TWHDX	Data Hold after $\overline{WR}$↑	40		0		ns	
TJLJH	Interrupt Request Width (Low)	100		100		ns	See Note 1
TCVIAH	Cascade Setup to Second or Third $\overline{INTA}$↓ (Slave Only)	55		55		ns	
TRHRL	End of $\overline{RD}$ to Next Command	160		160		ns	
TWHRL	End of $\overline{WR}$ to Next Command	190		190		ns	

Note: 1. This is the low time required to clear the input latch in the edge triggered mode.

TIMING RESPONSES

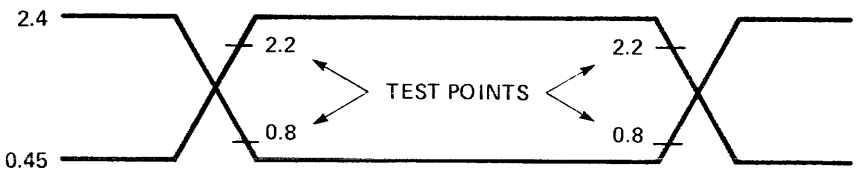
Symbol	Parameter	8259A-8 Min.	8259A-8 Max.	8259A Min.	8259A Max.	Units	Test Conditions
TRLDV	Data Valid from $\overline{RD}$/$\overline{INTA}$↓		300		200	ns	C of Data Bus = 100 pF
TRHDZ	Data Float after $\overline{RD}$/$\overline{INTA}$↑	20	200		100	ns	C of Data Bus Max. test C = 100 pF Min. test C = 15 pF
TJHIH	Interrupt Output Delay		400		350	ns	
TIAHCV	Cascade Valid from First $\overline{INTA}$↓ (Master Only)		565		565	ns	C_{INT} = 100 pF
TRLEL	Enable Active from $\overline{RD}$↓ or $\overline{INTA}$↓		160		125	ns	$C_{CASCADE}$ = 100 pF
TRHEH	Enable Inactive from $\overline{RD}$↑ or $\overline{INTA}$↑		325		150	ns	
TAHDV	Data Valid from Stable Address		350		200	ns	
TCVDV	Cascade Valid to Valid Data		300		300	ns	

CAPACITANCE

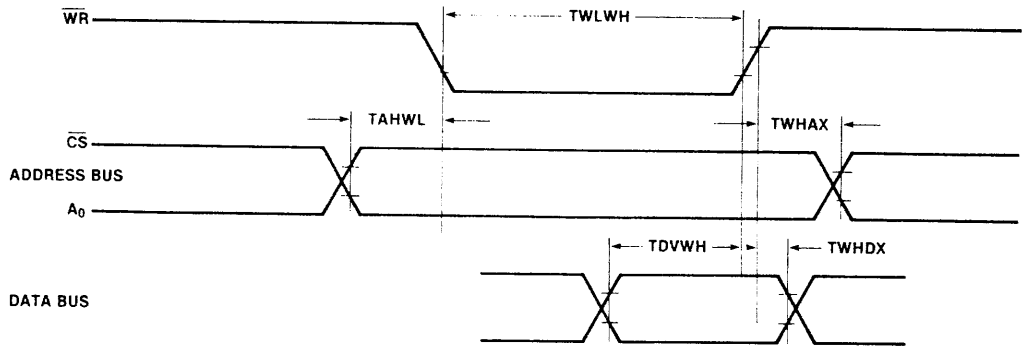
$T_A = 25°C$; $V_{CC} = GND = 0V$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	fc = 1 MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to V_{SS}

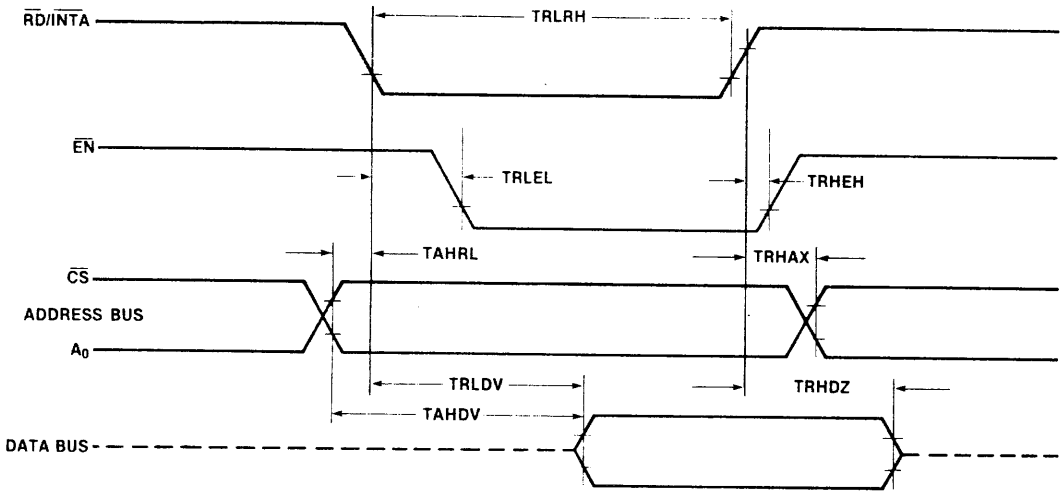
Input Waveforms for A.C. Tests



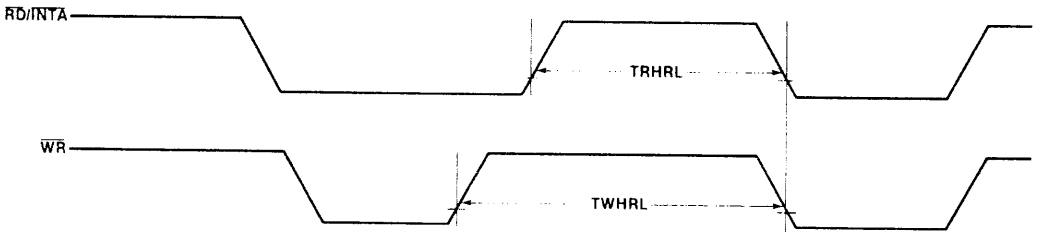
WRITE MODE



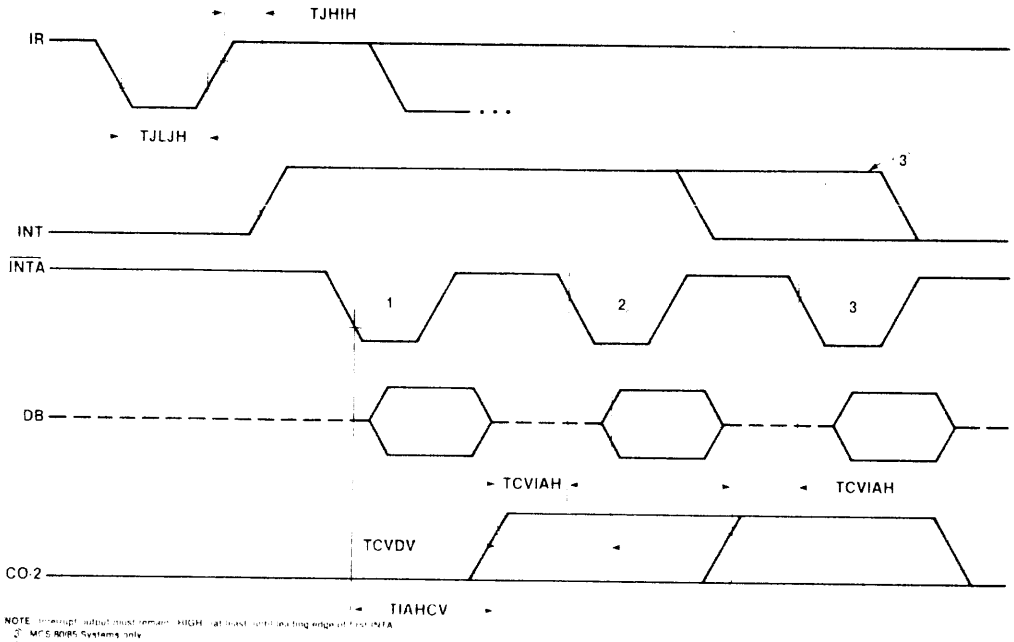
READ/INTA MODE



OTHER TIMING



INTA SEQUENCE



NOTE:

3. MCS-80/85 Systems only.

VERSATEC PRINTER/PLOTTER
GENERAL INTERFACE SPECIFICATIONS

APPENDIX C

VERSATEC
A XEROX COMPANY

Electrostatic Printer/Plotter Interface Specification

INTRODUCTION

The basic interface is the standard signal connection point for all Versatec printers, plotters, and printer/plotters. This bulletin provides a detailed technical description of the interface for all Versatec 8½, 11, and 20-inch electrostatic units; pin connection lists and timing diagrams are also provided. The information given here does not pertain to special computer interfaces, data communication interfaces, software, or special input codes.

Specifications on all Versatec electrostatic units, Versatec controllers, and Versaplot plotting software systems are available from the Versatec Marketing Department in Santa Clara, California.

GENERAL

Electrostatic writing is accomplished by programming the voltage applied to a stationary linear array of writing nibs which produce an invisible charge directly on the surface of dielectrically-coated paper. The charge is developed by a liquid toner which produces a permanent, high contrast visible image of the data received as the paper moves out of the machine (Figure 1).

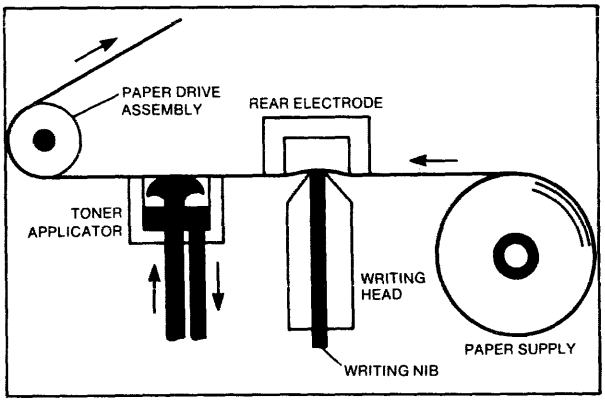


FIGURE 1. TYPICAL VERSATEC CONFIGURATION SHOWING PRINTER/PLOTTER OPERATION

Versatec printers accept asynchronous USASCII data in serial or parallel format. The ASCII input is decoded and converted to characters by means of a Read Only Memory (ROM) which is included in the standard configuration. Versatec plotters accept software-generated unweighted binary data in eight-bit bytes for raster scan plotting of graphic information. Each data bit relates to one nib in the plotting mode. Combination printer/plotters accept both printing and plotting input data.

Standard Versatec printers, plotters, and printer/plotters are supplied with both parallel and serial signal interfaces. The parallel interface accepts data in a bit parallel, character, or byte parallel mode. The serial interface accepts data in a bit serial, character, or byte serial mode.

PRINT OPERATIONS

Print operations are applicable to all Versatec printers and printer/plotters. Print data may be applied at either the parallel signal interface at connector J1, or the serial signal interface at connector J2 (see pin assignments, Figures 2 and 3). The PRINT input signal, applied at pin 12, J1, parallel signal interface, controls selection of PRINT or PLOT mode. When PRINT is HIGH and input clock, PICLK, is received, PRINT mode is selected. When PRINT is LOW and input clock, PICLK, is received, PLOT mode is selected. On printers or plotters only, this line is internally fixed to select the appropriate mode. The PRINT line can only be changed when the Versatec unit is ready.

The print input accepts ASCII seven or eight-level code in parallel or serial form. The selection of serial or parallel input may be made by logical selection at parallel input connector, J1, pin 13. This signal line, PARIN, must be held LOW for serial input or HIGH for parallel input. An open connection is interpreted as a HIGH.

The character generator in the Versatec printer contains a ROM which stores up to 256 characters. Characters are entered and stored in a line buffer. When the buffer is full (one line of characters) the line is automatically printed. If the buffer contains less than a full line of characters, a control command is required to initiate printing.

Control commands may be transmitted using the remote control lines described in Figure 4, or by transmitting the appropriate ASCII control code as shown in Figure 5. There are no ASCII control codes when the 128-character or larger set is used.

Automatic hardware line counting is provided for use with fan-fold paper. This feature provides automatic page separation and prevents printing on the perforated folds. When the page is full the paper will automatically advance to top of form. The line counter is reset by the form feed (FF), end of transmission (EOT), or reset control signals, as well as by entering the PLOT mode. Automatic line counting is disabled when operation with roll paper is selected via the ROLL/FAN-FOLD control switch, or when in the PLOT mode.

PLOT OPERATIONS

Plot operations are applicable to all Versatec plotters and printer/plotters. Plot input data are applied at the parallel interface at connector J1, or the serial interface at connector J2 shown in Figures 6 and 7, respectively.

Data consist of eight-bit binary unweighted bytes. For the number of bits per complete raster scan, refer to Table 1 on page 4.

J1 – Parallel input. Connector type: Cannon DCC-37P; Mating connector: Cannon DCC-37S. Twisted pairs not to exceed 50 feet.

	SIGNAL NAME	SIGNAL PIN NO.	SIGNAL COMMON PIN NO.	PAIR NO.	MNEMONICS
(Highest # Nib)	Input Bit 1 (LSB)	1	20	1	IN01
	Input Bit 2	2	21	2	IN02
	Input Bit 3	3	22	3	IN03
	Input Bit 4	4	23	4	IN04
	Input Bit 5	5	24	5	IN05
	Input Bit 6	6	25	6	IN06
	Input Bit 7	7	26	7	IN07
(Lowest # Nib)	Input Bit 8 (MSB)	8	27	8	IN08
	Clear	9	28	9	$\overline{\text{CLEAR}}$
	Parallel Input Clock	10	29	10	PICLK
	Ready	11	30	11	$\overline{\text{READY}}$
	Printer	12	31*	12	PRINT
	Parallel	13	31*	13	PARIN
	Simultaneous Print/Plot	14	33	14	$\overline{\text{SPP}}$
	Remote Reset	15	34	15	$\overline{\text{RESET}}$
	Remote Form Feed	16	35	16	$\overline{\text{RFFED}}$
	Remote End of Transmission	17	36	17	$\overline{\text{REOTR}}$
	Remote Line Terminate	18	37	18	$\overline{\text{RLTER}}$
	No Paper Sense	19**		19	NOPAP
	On-Line	32**			$\overline{\text{ONLIN}}$

*Two commons tied to pin 31 **No common for these two signals.

NOTE: There is no ground return provided for long line drivers and receivers.

FIGURE 2. PARALLEL SIGNAL INTERFACE CONNECTOR PIN ASSIGNMENTS

J2–Serial input. Connector type: Cannon DBC-25S; Mating connector: Cannon DBC-25P.

PIN	FUNCTION		REMARKS
	USED	NOT USED BUT TERMINATED	
1*	Protective Ground		Ground
2		Transmitted Data	Held At Mark
3	Received Data		Serial Data Input
4		Request To Send	Held At Mark
5		Clear To Send	Terminated To GND
6		Data Set Ready	Terminated To GND
7*	Signal Ground		Signal Common
8		Received Line Signal	Terminated To GND
12		Sec. Received Line Sig. Detect.	Terminated To GND
13		Sec. Clear To Send	Held At Mark
14		Sec. Transmitted Data	Held At Mark
15		DCE Source	Terminated To GND
19		Sec. Request To Send	Held At Mark
20		Data Terminal Ready	Held At Space
21		Sig. Quality Detect.	Terminated To GND
22		Ring Indicator	Terminated To GND
25**	Ready ($\overline{\text{SERDY}}$)		Serial Ready

*Pins 1 and 7 are connected internally

**Logic Level on Ready ($\overline{\text{SERDY}}$) is: High = +3.5V to 5V = BUSY
Low = –0.5V to +0.5V = READY

FIGURE 3. SERIAL SIGNAL INTERFACE CONNECTOR PIN ASSIGNMENTS

Remote control signals are used to control electrostatic unit operations. They apply to PRINT, PLOT, and SPP operations and facilitate remote control of a Versatec unit by a computer or other device.

SIGNAL NAME	SIGNAL MNEMONIC	SIGNAL REQUIRED	OPERATION
Clear	$\overline{\text{CLEAR}}$	Low Going Pulse, 300ns Min.	a. Clears Buffer when Matrix is in Data Entry Mode (when $\overline{\text{READY}}$ is LOW). b. Causes $\overline{\text{READY}}$ to go HIGH for 25 μs or less.
Remote Reset	$\overline{\text{RESET}}$	Low Going Pulse, 300ns Min.	a. Clears Buffer and initializes all logic. b. Causes $\overline{\text{READY}}$ to go HIGH for 25 μs or less. c. Will not reset out of paper.
Remote Line Terminate	$\overline{\text{RLTER}}$	Low Going Pulse, 300ns Min.	a. Forces Write Cycle. b. Causes $\overline{\text{READY}}$ to go HIGH for duration of write cycle. c. If in plot mode first $\overline{\text{RLTER}}$ after full buffer is ignored.
Remote Form Feed**	$\overline{\text{RFFED}}$	Low Going Pulse, 300ns Min.	a. Forces Write Cycle. b. With Fan-Fold Operation causes paper to advance to top of next page. c. With Roll Operation causes paper to advance approximately 2.5 inches. d. Causes $\overline{\text{READY}}$ to go HIGH until paper is advanced.
Remote End of Transmission*	$\overline{\text{REOTR}}$	Low Going Pulse, 300ns Min.	a. Forces Write Cycle. b. With Fan-Fold Operation causes paper to advance 8 inches, then to top of next page. c. With Roll Operation causes paper to advance approximately 8 inches. d. Causes $\overline{\text{READY}}$ to go HIGH until paper is advanced.

*Not to be asserted when in SPP and PRINT mode.
**If FF is issued while in fan-fold mode and unit is switched to ROLL, the Versatec unit will go out of paper.

FIGURE 4. REMOTE CONTROL SIGNALS

CONTROL SIGNAL NAME	ASCII CODE (OCTAL)	OPERATION		
EOT (End of Transmission)	004	Causes print cycle and paper advance of 8 inches, then stop if in roll mode, or continue advance to top of next page if in fan-fold mode. Do not use if in SPP mode.		
FF (Form Feed)	014	Causes print cycle and paper advance of 2-1/2 inches if in roll mode, or advance to top of next page if in fan-fold mode. Do not use if in SPP mode.		
LF (Line Feed)	012	Causes print cycle and paper advance of one line except when: 1. Follows print of a full buffer. 2. Follows a Carriage Return which causes a print cycle.		
CR (Carriage Return)	015	Causes print cycle and paper advance of one line, only if buffer has at least one character entered but is not full.		
DC1	021	When in serial mode, changes from print to plot mode for one scan.		
CR, LF	015, 012	**FB*** IGNORED, IGNORED	**PB*** WRITE, IGNORE	**EB*** IGNORE, WRITE

FIGURE 5. ASCII CONTROL CODES

*FB = Full Buffer; PB = Partial Buffer; EB = Empty Buffer.

Each dot corresponds to a single bit in the buffer. If a bit is "1", a black dot is plotted at the point corresponding to the bit position in the buffer. Input bit 8 (IN08) is the MSB and corresponds to the lowest numbered writing nib in each byte. For example, in the first byte transmitted, IN08 should address the first nib. Thus, IN01 of the last byte would address the last nib on the Versatec unit.

When the last byte is stored in the buffer, a single scan is automatically generated and one scan line of data points is plotted. A paper increment equal to the horizontal resolution is generated and the Versatec unit is then ready to plot another scan line of data points. Remote control signals are described in Figure 4.

($\overline{\text{RLTER}}$, $\overline{\text{RFFED}}$, $\overline{\text{REOTR}}$,) may be used to generate the scan if less than a full buffer is entered. The clear line ($\overline{\text{CLEAR}}$) may be used to clear the buffer prior to entering data.

Data may be entered (when $\overline{\text{READY}}$ is LOW) up to the maximum rate of 1 million bytes per second.

SIMULTANEOUS PRINT/PLOT (SPP) OPERATIONS

Simultaneous Print/Plot (SPP) operation is provided to permit direct overlaying of character data generated by the

internal character generator, with plotting data generated on a dot basis. This is an optional feature on some Versatec printer/plotters.

Printing and plotting data are entered in parallel format to input J1 from a computer or other data source. The internal character generator generates the appropriate character format from the input ASCII code.

Plotting data are entered as unweighted binary eight-bit bytes as described under Plot Operations.

When the plot buffer is filled or an $\overline{\text{RLTER}}$ is given, the plot buffer is scanned and a single row of dots which corresponds to the binary contents of the plot buffer is written.

During the scanning process, the print buffer is likewise scanned. The corresponding dot(s) of each character are OR'D with the plot buffer output, thus overlaying the printed and plotted data. NOTE: On Model 200A the printing buffer holds 70 characters maximum during SPP operation (see Table 1 below).

TABLE 1. MAXIMUM BUFFER LENGTH

Model	Print		Plot	
	Characters/ line	No. of scans 64/96, 128*	Bits	Bytes
200A	80 (70 SPP)	8/10	560	70
800	100	10/12	800	100
900	100	20/20	1600	200
1100	132	10/12	1024	128
1200	132	20/20	2112	264
1600	100	20/20	1600	200
2000	232	10/12	1856	232
2030	232	10/12	1856	232
2160	180	20/20	2880	360

The $\overline{\text{SPP}}$ mode is controlled by a single input line, $\overline{\text{SPP}}$. When $\overline{\text{SPP}}$ is LOW, only parallel data bytes are accepted and the Versatec unit operates only in the SPP mode.

If the PRINT control line is LOW, the data byte is stored in the plot buffer. If PRINT is HIGH the data byte is stored in the print buffer. Remote or ASCII control codes, EOT (End of Transmission), or FF (Form Feed) are illegal codes in the SPP mode when the PRINT control line is HIGH. When the PRINT control line is LOW, i.e., in PLOT mode, the remote control line, $\overline{\text{REOTR}}$, functions as described in Figure 4.

*NOTE: The number of scans value listed is the minimum value for standard characters. A maximum of 32 scans may be required for oversized and special characters.

Normal operation consists of first filling the print buffer. This is accomplished by placing the PRINT line HIGH, in the SPP mode, and entering characters. If the buffer is not filled, the line may be terminated by a CR or LF code. The $\overline{\text{READY}}$ line now goes to the busy state, indicating that the buffer is full. The PRINT line is now placed LOW, indicating PLOT mode. This causes the $\overline{\text{READY}}$ line to go LOW indicating the plot buffer can be filled. Unweighted binary plot data are now loaded into the plot buffer, one byte at a time, until the plot buffer is full or an $\overline{\text{RLTER}}$ is given. The $\overline{\text{READY}}$ line now goes busy again and a single scan is generated. Note that the writing process is controlled by the plot buffer. An input clock is required when changing from PRINT to PLOT.

To completely print the line in the print buffer, a number of scans must be plotted. New data can be entered into the print buffer after the last scan of the previous line of characters is completed.

Operation of the Control Lines in the SPP mode is as shown in Table 2.

SPP OPTION FOR 1100A, 96/128-CHARACTER SET

In the SPP mode the Versatec unit becomes a raster scan plotter with a hardware-generated print capability. That is, a write cycle can only be caused by terminating the plot buffer which will generate one scan. ASCII-generated Form Feed (FF) and End of Transmission (EOT) characters will not be honored.

For example, in the following routine we will overlay the print character "A" and a diagonal line plotted left to right and examine it step by step:

Step 1. Set Print

Step 2. Set SPP

TABLE 2. CONTROL LINE OPERATION, SPP MODE

SIGNAL NAME	SIGNAL LEVEL	OPERATION
PRINT	HIGH	Causes parallel data bytes to be loaded into print buffer. $\overline{\text{READY}}$ indicates status of print buffer.
	LOW	Causes parallel data bytes to be loaded into plot buffer. $\overline{\text{READY}}$ indicates status of plot buffer.
$\overline{\text{SPP}}$	HIGH	Normal machine operation.
	LOW	SPP mode, parallel data only.
$\overline{\text{CLEAR}}$	Negative Going Pulse 300 ns Min.	Clears plot buffer (plot mode) or print buffer (print mode).
$\overline{\text{RESET}}$	Negative Going Pulse 300 ns Min.	Clears both print and plot buffer, resets all logic.

Step 3. Send the following ASCII data:

SPACE	SPACE	"A"	Line Feed
$(040)_8$	$(040)_8$	$(101)_8$	$(012)_8$

Step 4. Set Plot

Step 5. Send the following Plot data (MSB=Bit 8)

$(200)_8$	$(000)_8$	LTER	=	Scan 1
$(100)_8$	$(000)_8$	LTER	=	Scan 2
$(040)_8$	$(000)_8$	LTER	=	Scan 3
$(020)_8$	$(000)_8$	LTER	=	Scan 4
$(010)_8$	$(000)_8$	LTER	=	Scan 5
$(004)_8$	$(000)_8$	LTER	=	Scan 6
$(002)_8$	$(000)_8$	LTER	=	Scan 7
$(001)_8$	$(000)_8$	LTER	=	Scan 8
$(000)_8$	$(200)_8$	LTER	=	Scan 9
$(000)_8$	$(100)_8$	LTER	=	Scan 10
$(000)_8$	$(040)_8$	LTER	=	Scan 11
$(000)_8$	$(020)_8$	LTER	=	Scan 12

Step 1 and 2
As far as the Versatec unit is concerned, it isn't necessary to be in the PRINT mode to set SPP. However, this is the sequence that must be followed with many of our controllers.

Once SPP is set it isn't necessary to switch in and out of SPP mode unless you wish to use the unit as a printer only.

Step 3
There is a two-space character prior to the "A" because the Plot width is four bytes narrower and centered with respect to Print.

When the print buffer is terminated (ASCII LF or CR or RLTER) or filled (132 print bytes) $\overline{\text{READY}}$ will indicate busy until the print buffer is cleared, the unit is reset, or the print cycle has been completed.

The function of the READY line is to indicate the status of the buffer being selected. Since the print buffer has been terminated and has not completed writing its contents, $\overline{\text{READY}}$ will indicate busy as long as Print is set (indicating the print buffer is not ready to receive data).

Step 4
When Plot is set, $\overline{\text{READY}}$ will go true (indicating the plot buffer is ready to receive data).

Step 5
Each time the plot buffer is terminated or filled, the Versatec unit will indicate busy until is has plotted the contents of the plot buffer and OR'D with the contents of the print buffer as decoded by the character generator for that particular scan.

After generating 12 plot scans, the print buffer will have completed the writing cycle and may again be selected.

PARALLEL SIGNAL INTERFACE

The parallel signal interface is used to receive parallel input data and control signals. It is used whenever high speed data transfer is required, as with a standard computer I/O data bus.

The parallel signal interface consists of eight data lines and 12 control lines. Figure 2 lists the connector pin assignments. Positive logic, TTL or DTL-compatible levels are used.

The ready line ($\overline{\text{READY}}$) indicates the current status of the Versatec unit. The unit is busy when $\overline{\text{READY}}$ is HIGH. Figure 6 shows the normal operation of the ready line during receipt of data. $\overline{\text{READY}}$ remains at the busy level for longer intervals while the Versatec unit is printing or plotting.

Data are accepted on eight lines (IN01-IN08). Data can only be entered when $\overline{\text{READY}}$ is LOW. Data consist of character codes or control codes as defined in Figure 8, Versatec ASCII Character Set, and Figure 5, ASCII Control Codes.

A parallel input clock pulse (PICLK) is required for each byte of input data. Figure 6 shows the timing relationship between the clock and the data signal. Clock pulses should be transmitted when $\overline{\text{READY}}$ is LOW. The maximum data transfer rate is 1 million eight-bit bytes per second.

The signal level on the printer line (PRINT) determines, in the case of printer/plotters only, whether the Versatec unit functions as a printer or a plotter. If PRINT is HIGH the unit functions as a PRINTER. An open line will be interpreted as a HIGH. If PRINT is LOW the unit functions as a plotter. For printer only or plotter only, the mode is determined internally.

Printer/plotters will write the data on paper in the mode last set (i.e., if "N" ASCII characters were entered into the buffer in the PRINT mode and the mode was then changed to PLOT and if the remainder of the buffer was filled with plot data or a RLTER or REOTR was issued, the entire buffer will be plotted rather than printed).

The signal level on the on-line ($\overline{\text{ONLIN}}$) is LOW when the Versatec unit power is on. A tie-up resistor must be provided by the user on this line to maintain a HIGH level when power is off, or the input cable is disconnected.

The no paper sense line (NOPAP) is HIGH if the paper supply is depleted. The red warning indicator, PAPER, on the control panel also lights to indicate the out-of-paper condition. A tie-up resistor must be provided by the user on this line to maintain a HIGH level when power is off, or the input cable is disconnected.

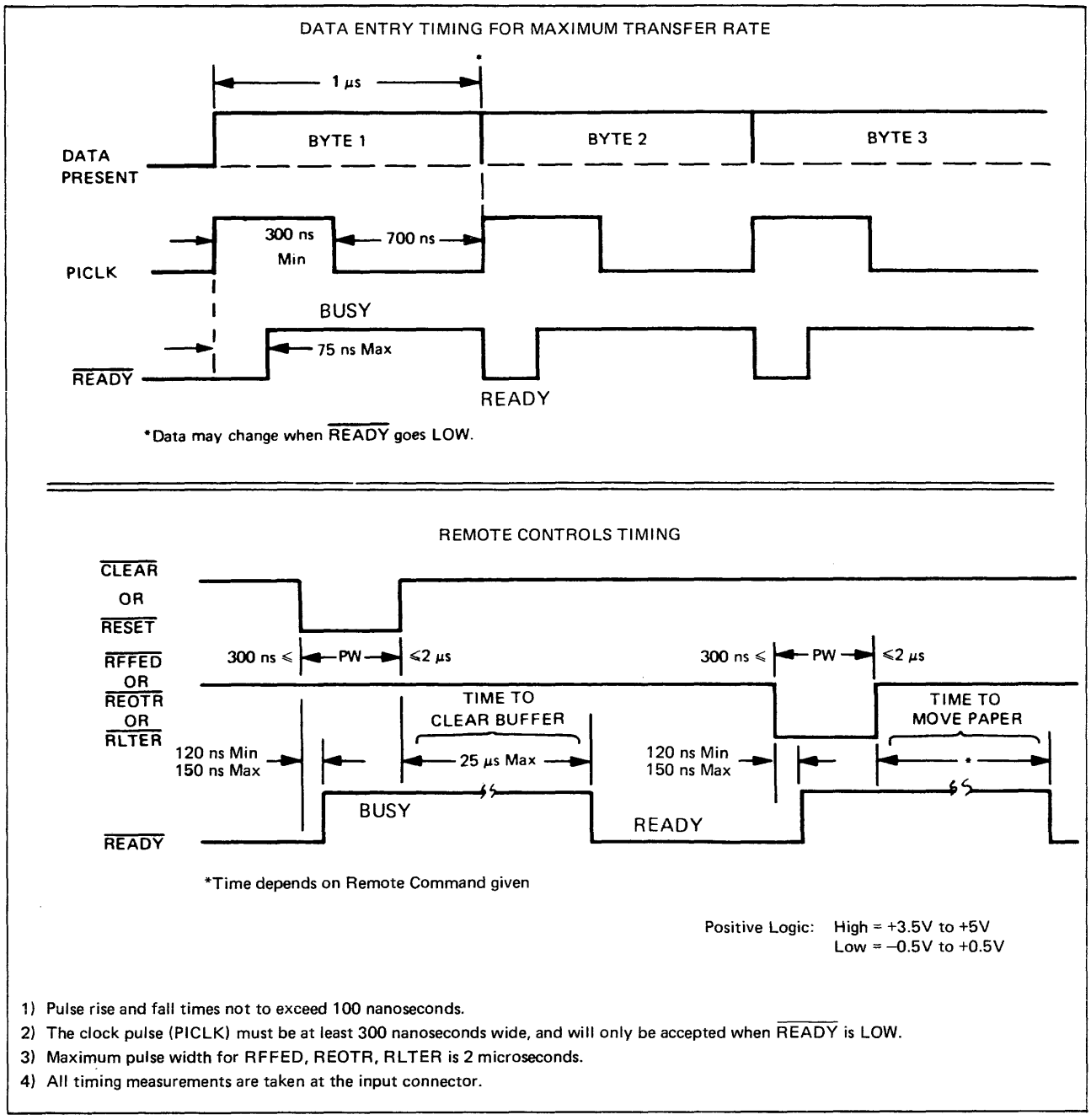
The simultaneous print/plot line ($\overline{\text{SPP}}$) is HIGH in normal operation. When LOW, SPP operation is indicated and only parallel data are accepted. The print line determines whether data bytes will be loaded into the print or plot buffer (SPP machines only). If the SPP option is not provided, this line is inoperative.

Operation of additional remote control lines is described in Figure 4.

SERIAL SIGNAL INTERFACE

The serial signal interface is used to receive asynchronous serial data. Either printing or plotting data may be received.

The serial signal interface may receive data if the input control line, PARIN, on J1, pin 13 (parallel signal interface) is LOW. This may be accomplished by using the supplied 37-pin parallel connector with pins 10 (PICLK) and 13 (PARIN) tied to pin 31 (GND). The serial signal interface



1) Pulse rise and fall times not to exceed 100 nanoseconds.
2) The clock pulse (PICLK) must be at least 300 nanoseconds wide, and will only be accepted when $\overline{\text{READY}}$ is LOW.
3) Maximum pulse width for RFFED, REOTR, RLTER is 2 microseconds.
4) All timing measurements are taken at the input connector.

FIGURE 6. PARALLEL SIGNAL INTERFACE

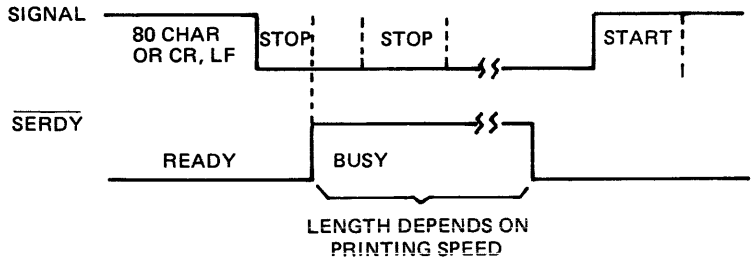
consists of two signal lines and a ready line. The remaining 13 RS 232C control lines are not used but are terminated in the Versatec unit.

The received data line is the input line for level shift, bit serial, character or byte serial data. The signal ground line is the data return line. All lines except serial ready ($\overline{\text{SERDY}}$) are negative logic, Teletype-compatible levels as described in Figure 3. If specified at time of order, positive logic, TTL-compatible levels may be supplied for all lines.

Pin assignments and negative logic voltage levels are compatible with EIA Standard RS232C.

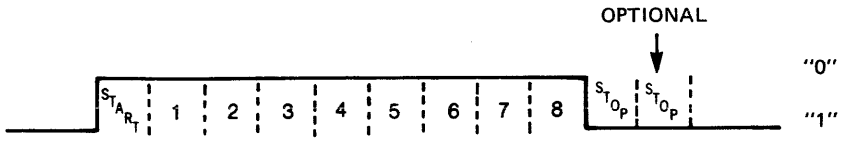
A serial ready line ($\overline{\text{SERDY}}$) is provided and it is recommended that data be entered only when $\overline{\text{SERDY}}$ is LOW. Data entered when $\overline{\text{SERDY}}$ is HIGH are lost. $\overline{\text{SERDY}}$ goes HIGH upon receipt of a full buffer on a Carriage Return (CR) or Line Feed (LF) code. Timing is shown in Figure 7. $\overline{\text{SERDY}}$ is connected to a normally unassigned pin on the EIA RS232C standard interface and the voltage levels are +5 volts for HIGH and 0 volts for LOW.

In single buffer units, data cannot be received while the machine is printing or plotting. After receipt of a LF or CR or a full buffer, the data transmitting source must not transmit while the Versatec unit is printing or plotting. In addition, for both single buffer and dual buffer Versatec models, a waiting time of approximately 2 seconds must be observed for the first print line or plot scan to allow toner to reach the toner channel. If no printing or plotting occurs for a period of 1.5 seconds or more, this waiting time must again be observed by the transmitting data source.



NOTE:

1) Positive or negative logic should be specified at time of order. Negative logic is supplied unless otherwise specified.
2) Signal positions 1-8 (see timing diagram) contain bits 1-8. Bit 1 is the LSB (least significant bit). Bit 8 is the MSB (most significant bit).
3) The second stop position is optional. Either 10 or 11 element codes are acceptable.



BIT ASSIGNMENT – SERIAL ASCII

STANDARD

Negative BI POLAR Logic
"1" (true) = –5V to –25V (MARK)
"0" (false) = +5V to +25V (SPACE)

OPTIONS

Positive BI POLAR Logic
"0" (true) = –5V to –25V (MARK)
"1" (false) = +5V to +25V (SPACE)

Positive TTL Logic
"1" (true) = +3.5V to +5V (+5V nominal)
"0" (false) = –0.5V to +0.5V (0V nominal)

FIGURE 7. SERIAL SIGNAL INTERFACE DATA ENTRY TIMING

The characters shown below are standard for Versatec models: LP-810, LP-960, LP-1150, LP-1175, LP-1616, LP-1250, 2000A and 2030A. There are four character variations for models LP-960, LP-1616 and LP-1250. These variations are given on the right side of the four boxes which contain two different characters.

BIT 4	BIT 3	BIT 2	BIT 1	BIT 7	0	0	0	0	0	0	1	1	1	1
				BIT 6	0	0	0	0	1	1	0	0	1	1
				BIT 5	0	1	0	1	0	1	0	1	0	1
0	0	0	0		+	α		*	SPACE	Ø	@	P	◣	p
0	0	0	1		±	DCL		DCL	!	1	A	Q	a	q
0	0	1	0		×	β		*	"	2	B	R	b	r
0	0	1	1		≠	γ		*	#	3	C	S	c	s
0	1	0	0		EOT	Δ	EOT	*	$	4	D	T	d	t
0	1	0	1		∂	ε		*	%	5	E	U	e	u
0	1	1	0		∞	θ		*	&	6	F	V	f	v
0	1	1	1		∈	λ		*	'	7	G	W	g	w
1	0	0	0		≤	μ		*	(	8	H	X	h	x
1	0	0	1		≥	ν		*	)	9	I	Y	i	y
1	0	1	0		LF	π	LF	*	*	:	J	Z	j	z
1	0	1	1		°	ρ		*	+	;	K	[	k	{
1	1	0	0		FF	Σ	FF	*	,	<	L	\	l	¦ |
1	1	0	1		CR	σ	CR	*	–	=	M	]	m	}
1	1	1	0		′	φ		*	.	>	N	↑ ^	n	~
1	1	1	1		″	ψ		*	/	?	O	← _	o	■

124 SCIENTIFIC CHARACTER SET (OPTIONAL) **

64 CHARACTER SET

96 CHARACTER SET (OPTIONAL)

LEGEND

EOT END OF TRANSMISSION
LF LINE FEED
FF FORM FEED
CR CARRIAGE RETURN
DC1 STANDARD CODE FOR SERIAL PRINT TO PLOT MODE CHANGE

NOTE: EMPTY SPACES ARE UNASSIGNED AND IGNORED.

*optional codes for serial print/plot mode change.

**These two columns not used with 124 character set.

FIGURE 8. VERSATEC CHARACTER SETS

Serial inputs may be applied at rates from 110 to 9600 BPS synchronous by bit and asynchronous by character or byte. Each character or byte consists of 10 or 11 elements as shown in Figure 7. The first bit is the start bit which causes the clock in the printer to start and run at a predetermined rate. The rate is determined by the placement of a jumper wire on the Input Logic PC board. The rate can be set for 9600, 4800, 2400, 1200, 600, 300, 150, and 110 BPS. The maximum rate is 19,200 BPS on 2030 and 1110A models. The next eight bits contain the data code. The character code accepted for print data is ASCII. Plotting data are unweighted binary. The stop bits are ignored. Printing operations are as described earlier, except that remote control lines are not used. The print mode of operation is normally selected. Plotting mode may be selected by entering an ASCII control character, DC1, 021 (OCTAL). This control code must be transmitted as the first byte preceding plotting data. At the completion of the scan, the Versatec unit reverts to the printing mode. Printing or plotting at very slow rates may cause poor print quality due to overdevelopment of the image. Therefore, printing serially at low rates, below 600 BPS, is not recommended. Likewise, plotting serially at less than 2400 BPS is not recommended.

CONTROLLERS FOR OPERATING VERSATEC UNITS

Versatec controllers are available for the computers listed below. For complete specifications on each model, refer to the separate Versatec data sheets on controllers. Controllers and special interface designs for other equipment will be quoted on request.

- Data General NOVA and Super NOVA series.
- Digital Equipment Corporation PDP8, PDP11, PDP12, and PDP9/15.
- Hewlett-Packard 2100, 2114, 2115, 2116, 2100A, 2100S, 21MX.
- Varian 620 and 73.
- Xerox Data Systems Sigma series.
- Honeywell 316 and 516.
- Interdata 70, 74, 80, 85, 6/16, 7/16, 7/32 and 8/32.
- IBM 360, 370, 1130.
- Digital Computer Controls D116 series.
- ROLM computers.

LONG LINE DRIVERS AND RECEIVERS (See Figure 9)

Differential line drivers and receivers are used in both controllers and Versatec units to enable long line communications. The interface cables may be twisted (#24-gauge stranded wire) cable. The Versatec I/O circuits for cable lengths greater than 50 feet but less than 1500 feet are shown in Figure 10.

The signals which are not differentially activated are ONLIN and NOPAP. The driver for these signals is a TTL 7437 buffer circuit for which the controller receiver is a resistor terminator network and TTL load.

The schematic below describes the typical input and output circuits provided by Versatec electrostatic units. Input signals are applied to a typical receiver. Output signals are driven from a typical driver. Interface cables are limited to 50 feet in length, twisted pair, two twists per inch, #24 gauge stranded wire.

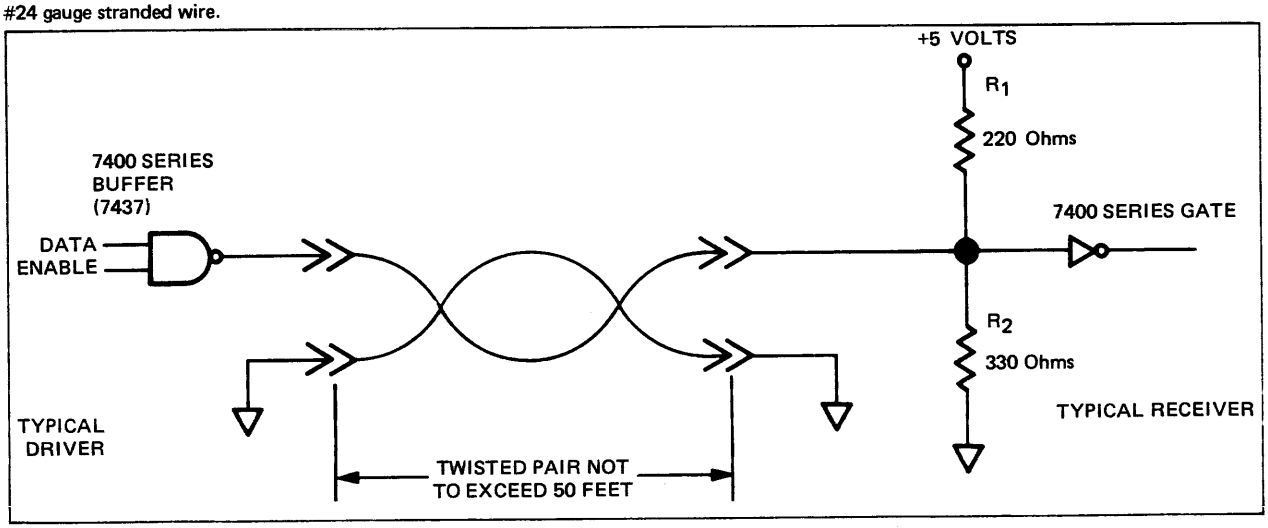


FIGURE 9. TYPICAL CABLE DRIVERS AND RECEIVERS

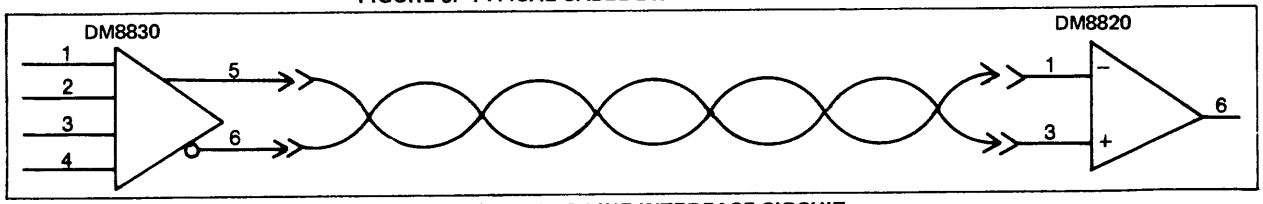


FIGURE 10. LONG LINE INTERFACE CIRCUIT

VERSATEC
A XEROX COMPANY
2805 Bowers Avenue
Santa Clara, California 95051
(408) 988-2800
TWX: 910-338-0243

Bulletin No. 312, September 1977 Printed in U.S.A.

PIN ASSIGNMENTS FOR TTL SIGNAL PARALLEL INTERFACE

	Signal Name	Signal Mnemonics	Signal Pin No.	Signal Common Pin No.	Pair No.
Right Most Nib	Input Bit 1 (LSB)	IN01	1	20	1
	Input Bit 2	IN02	2	21	2
	Input Bit 3	IN03	3	22	3
	Input Bit 4	IN04	4	23	4
	Input Bit 5	IN05	5	24	5
	Input Bit 6	IN06	6	25	6
	Input Bit 7	IN07	7	26	7
Left Most Nib	Input Bit 8	IN08	8	27	8
	Clear	$\overline{\text{CLEAR}}$	9	28	9
	Parallel Input Clock	PICLK	10	29	10
	Ready	$\overline{\text{READY}}$	11	30	11
	Printer	PRINT	12	31[1]	12
	Parallel	PARIN	13	31[1]	13
	Simultaneous Print/Plot	$\overline{\text{SPP}}$	14	33	14
	Remote Reset	$\overline{\text{RESET}}$	15	34	15
	Remote Form Feed	$\overline{\text{RFFED}}$	16	35	16
	Remote End of Transmission	$\overline{\text{REOTR}}$	17	36	17
	Remote Line Terminate	$\overline{\text{RLTER}}$	18	37	18
	No Paper Sense	NO PAP	19[2]		19
	On Line	$\overline{\text{ON LINE}}$	32[2]		

PIN ASSIGNMENTS FOR DIFFERENTIAL SIGNAL PARALLEL INTERFACE

	Signal Name	Signal Mnemonics (+ = Active High) (- = Active Low)	Pin No.
Right Most Nib	Input Bit 1 (LSB)	+ IN01	1
	Input Bit 2	+ IN02	2
	Input Bit 3	+ IN03	3
	Input Bit 4	+ IN04	4
	Input Bit 5	+ IN05	5
	Input Bit 6	+ IN06	6
	Input Bit 7	+ IN07	7
Left Most Nib	Input Bit 8	+ IN08	8
	Clear	-CLEAR	9
	Parallel Input Clock	+ PICLK	10
	Ready	-READY	11
	Printer	+ PRINT	12
	(Unused)	OPEN	13
	Simultaneous Print/Plot	-SPP	14
	Remote Reset	-RESET	15
	Remote Form Feed	-RFFED	16
	Remote End of Transmission	-REOTR	17
	Remote Line Terminate	-RLTER	18
	Inoperative	+ INOP	19

PIN ASSIGNMENTS FOR DIFFERENTIAL SIGNAL PARALLEL INTERFACE
(Continued)

Signal Name	Signal Mnemonics (+ = Active High) (- = Active Low)	Pin No.
Input Bit 1	- IN01	20
Input Bit 2	- IN02	21
Input Bit 3	- IN03	22
Input Bit 4	- IN04	23
Input Bit 5	- IN05	24
Input Bit 6	- IN06	25
Input Bit 7	- IN07	26
Input Bit 8	- IN08	27
Clear	+CLEAR	28
Parallel Input Clock	- PICLK	29
Ready	+READY	30
Printer	- PRINT	31
Inoperative	- INOP	32
Simultaneous Print/Plot	+SPP	33
Remote Reset	+RRSET	34
Remote Form Feed	+RFFED	35
Remote End of Transmission	+REOTR	36
Remote Line Terminate	+RLTER	37

PIN ASSIGNMENTS FOR PARALLEL INTERFACE

NOTES:

1) Two commons tied to pin 31.

2) No common for these two signals.

3) Parallel signal is held high internally for differential configuration. Pin 13 is inactive at the connector.

4) Parallel common Pin becomes reference Pin for PRINT signal line in differential configuration.

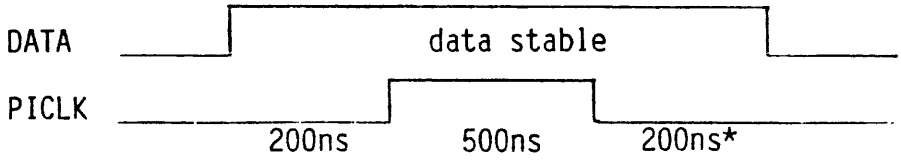
5) ON LINE and NO PAPER TTL signals are combined to provide a single inoperative (INOP) status signal in the differential configuration (i.e. the NOPAP pin becomes +INOP pin and the ONLIN pin becomes-INOP). INOP is active for either condition of NO PAPER or OFF LINE of the printer/plotter.

I/O PORT TIMING

APPENDIX D

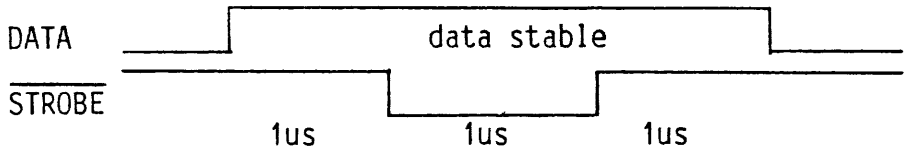
I/O PORT TIMING

VERSATEC PORTS

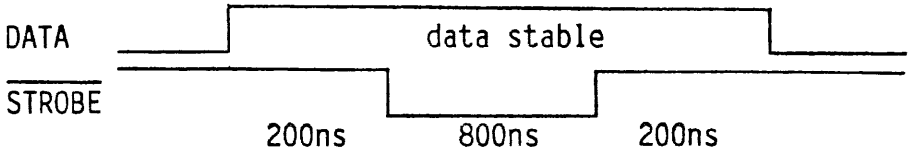


*or until $\overline{\text{READY}}$ re-asserted--depending on DMA request option selected

OPTION PORT normal timing



OPTION PORT compressed timing



OPTION PORT TO CENTRONICS
CABLE RUN LIST

APPENDIX E

10085 OPTION PORT TO "CENTRONICS"

Cable Run List

J1	"Centronics" Connector	Signal Function
1	1	$\overline{\text{STROBE}}$
2	19	GND
3	2	DATA 1
4	20	GND
5	3	DATA 2
6	21	GND
7	4	DATA 3
8	22	GND
9	5	DATA 4
10	23	GND
11	6	DATA 5
12	24	GND
13	7	DATA 6
14	25	GND
15	8	DATA 7
16	26	GND
17	9	DATA 8
18	27	GND
19	10	$\overline{\text{ACKNLG}}$
20	28	GND
21	11	BUSY
22	29	GND
23	12	PE
24	30	GND
25	13	SLCT
26	31	$\overline{\text{INPUT PRIME}}$
27	14	(NC)
28	32	$\overline{\text{FAULT}}$
29	15	(NC)
30	33	(NC)
31	16	(NC)
32	34	(NC)
33	17	(NC)
34	35	(NC)
	18	(NC) OPTIONAL FRAME GND
	36	(NC)

VERSATEC PORT CABLE RUN LIST

APPENDIX F

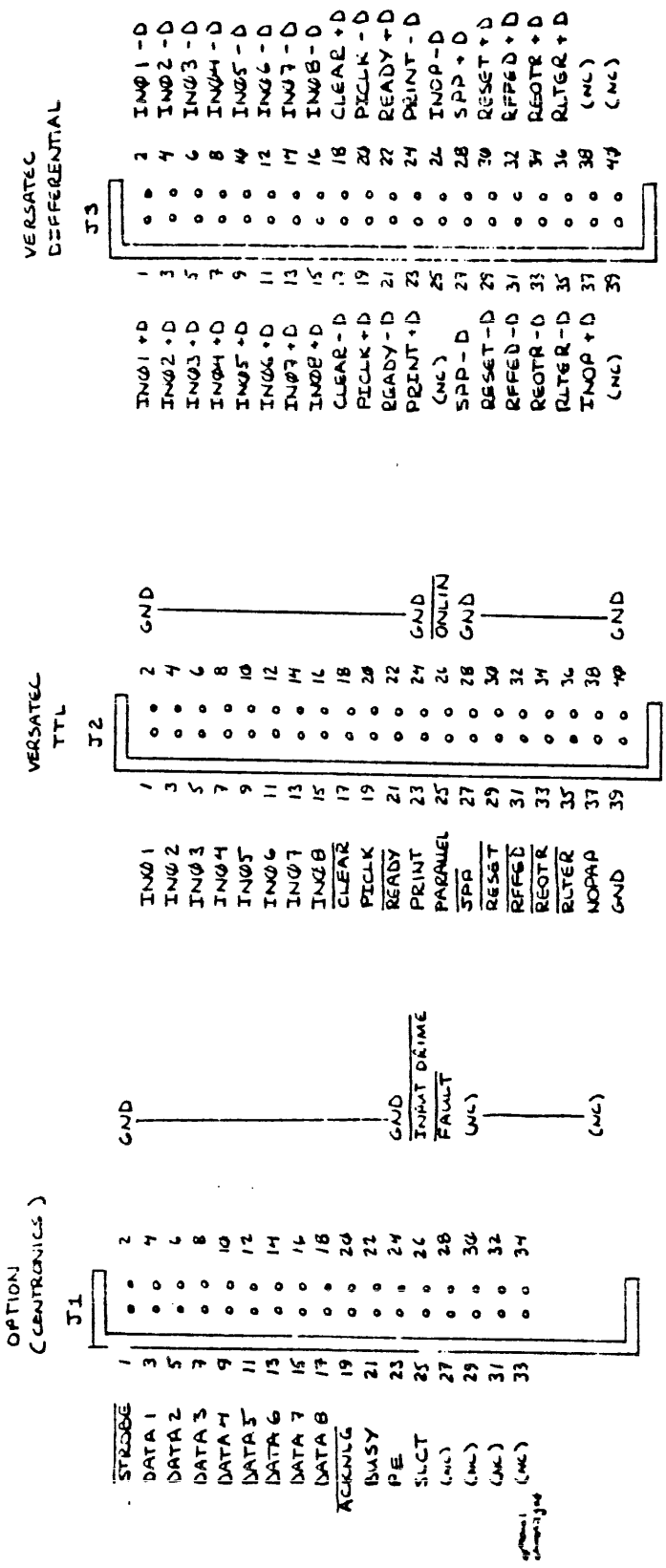
VERSATEC CABLE RUN LIST

J1 and J2 40-pin Headers	Signal Name TTL	Differential	37-pin "D" Plotter
1	IN01	IN01+D	1
2	GND	IN01-D	20
3	IN02	IN02+D	2
4	GND	IN02-D	21
5	IN03	IN03+D	3
6	GND	IN03-D	22
7	IN04	IN04+D	4
8	GND	IN04-D	23
9	IN05	IN05+D	5
10	GND	IN05-D	24
11	IN06	IN06+D	6
12	GND	IN06-D	25
13	IN07	IN07+D	7
14	GND	IN07-D	26
15	IN08	IN08+D	8
16	GND	IN08-D	27
17	$\overline{\text{CLEAR}}$	CLEAR-D	9
18	GND	CLEAR+D	28
19	PICLK	PICLK+D	10
20	GND	PICLK-D	29
21	$\overline{\text{READY}}$	READY-D	11
22	GND	READY+D	30
23	PRINT	PRINT+D	12
24	GND	PRINT-D	31
25	PARALLEL	N/C	13
26	$\overline{\text{ONLIN}}$	INOP-D	32
27	$\overline{\text{SPP}}$	SPP-D	14
28	GND	SPP+D	33
29	$\overline{\text{RESET}}$	RESET-D	15
30	GND	RESET+D	34
31	$\overline{\text{RFFED}}$	RFFED-D	16
32	GND	RFFED+D	35
33	$\overline{\text{REOTR}}$	REOTR-D	17
34	GND	REOTR+D	36
35	$\overline{\text{RLTER}}$	RLTER-D	18
36	GND	RLTER+D	37
37	NOPAP	INOP+D	19
38	GND		
39	GND		
40	GND		

*Note: PARALLEL is pulled up at the interface by a 220Ω resistor to +5v

I/O CONNECTOR PIN-OUTS

APPENDIX G


OPTION
(CENTRONICS)
J1
STROBE
DATA 1
DATA 2
DATA 3
DATA 4
DATA 5
DATA 6
DATA 7
DATA 8
ACKNLG
BUSY
PE
SLCT
(NC)
(NC)
(NC)
GND
GND
INPUT PRIME
FAULT
(NC)
(NC)
VERSATEC
TTL
J2
INØ1
INØ2
INØ3
INØ4
INØ5
INØ6
INØ7
INØ8
CLEAR
PICLK
READY
PRINT
PARALEL
SPP
RESET
RFFED
REOTR
RLTER
NOPAP
GND
GND
GND
ONLIN
GND
GND
VERSATEC
DIFFERENTIAL
J3
INØ1 +D
INØ2 +D
INØ3 +D
INØ4 +D
INØ5 +D
INØ6 +D
INØ7 +D
INØ8 +D
CLEAR -D
PICLK +D
READY -D
PRINT +D
(NC)
SPP -D
RESET -D
RFFED -D
REOTR -D
RLTER -D
INOP +D
(NC)
INØ1 -D
INØ2 -D
INØ3 -D
INØ4 -D
INØ5 -D
INØ6 -D
INØ7 -D
INØ8 -D
CLEAR +D
PICLK -D
READY +D
PRINT -D
INOP -D
SPP +D
RESET +D
RFFED +D
REOTR +D
RLTER +D
(NC)
(NC)